PICO-IMX8M-MINI
Reference User Manual

V1. 202003

Boardcon Embedded Design

www. boardcon. com

1. Introduction

1.1. About this Manual

This manual is intended to provide the user with an overview of the board and benefits, complete features specifications, and set up procedures. It contains important safety information as well.

1.2. Feedback and Update to this Manual

To help our customers make the most of our products, we are continually making additional and updated resources available on the Boardcon website (www.boardcon.com , www.armdesigner.com).

These include manuals, application notes, programming examples, and updated software and hardware. Check in periodically to see what's new!

When we are prioritizing work on these updated resources, feedback from customers is the number one influence, If you have questions, comments, or concerns about your product or project, please no hesitate to contact us at support@armdesigner.com.

1.3. Limited Warranty

Boardcon warrants this product to be free of defects in material and workmanship for a period of one year from date of buy. During this warranty period Boardcon will repair or replace the defective unit in accordance with the following process:

A copy of the original invoice must be included when returning the defective unit to Boardcon. This limited warranty does not cover damages resulting from lighting or other power surges, misuse, abuse, abnormal conditions of operation, or attempts to alter or modify the function of the product.

This warranty is limited to the repair or replacement of the defective unit. In no event shall Boardcon be liable or responsible for any loss or damages, including but not limited to any lost profits, incidental or consequential damages, loss of business, or anticipatory profits arising from the use or inability to use this product.

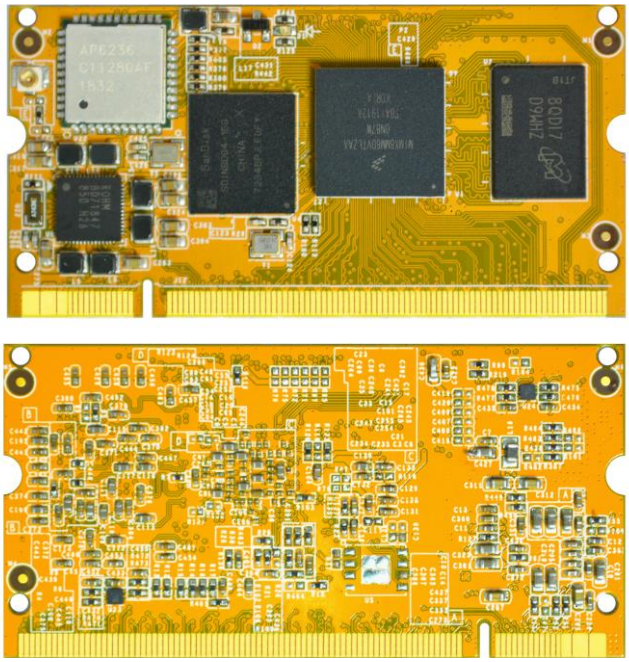
Repairs make after the expiration of the warranty period are subject to a repair charge and the cost of return shipping. Please contact Boardcon to arrange for any repair service and to obtain repair charge information.

Content

1 PICO-IMX8M-MINI Introduction

1.1 Summary

The PICO-IMX8M-MINI system-on-module is equipped with NXP's IMX8MINI quad Arm® Cortex®-A53 core, which operates at speeds of up to 1.8 GHz and A general purpose Cortex®-M4 400 MHz core processor is for low-power processing. It is designed specifically such as intelligent lamp post, advertising machine, new retail vending / ticketing machine, human-computer interactive query and business processing machine, high-performance instruments (industrial and medical), industrial control and human-computer interactive device, intelligent communication, intelligent fire protection, intelligent city, intelligent-building



1.2 Processor Features

SPECIFICATIONS	
CPU	• 4x Cortex-A53 core platforms up to 1.8GHz per core • 32KB L1-I Cache/ 32 kB L1-D Cache • 512 kB L2 Cache • 1x Cortex-M4 core up to 400MHz • 16 kB L1-I Cache/ 16 kB L2-D Cache
GPU	3D GPU (1x shader, OpenGL® ES 2.0) 2D GPU

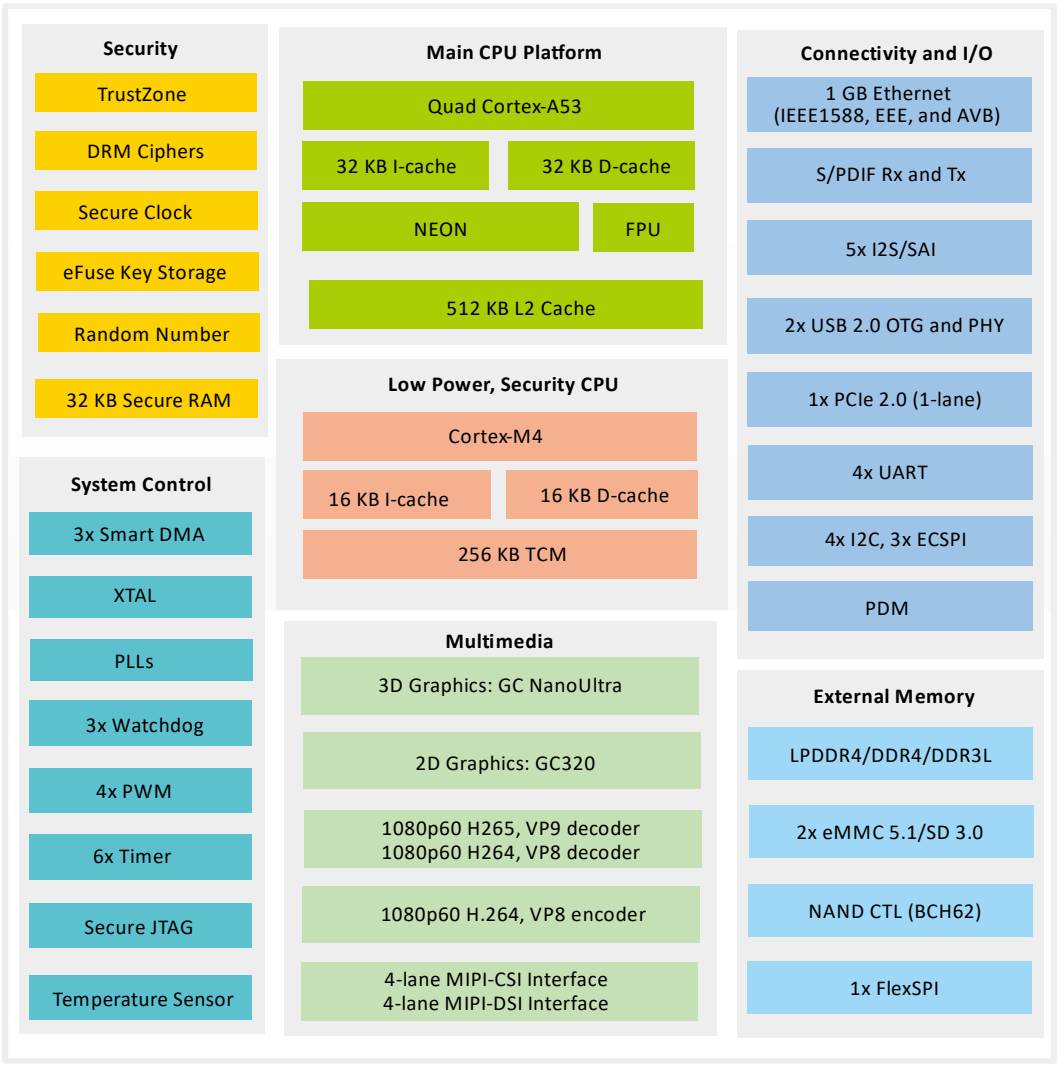
Display	1x MIPI DSI (4-lane) with PHY
Video Playback	1080p60 VP9 Profile 0, 2 (10-bit) decoder, HEVC/H.265 decoder, AVC/H.264 Baseline, Main, High decoder, VP8 decoder
	1080p60 AVC/H.264 encoder, VP8 encoder
Audio	5x SAI (12Tx + 16Rx external I2S lanes), 8ch PDM input
Camera	1x MIPI CSI (4-lane) with PHY
USB	2x USB 2.0 OTG controllers with integrated PHY
PCIe	1x PCIe 2.0 (1-lane) with L1 low power substates
Ethernet	RGMII interface
Temperature	0°C to 70°C

1.3 SoM Specifications

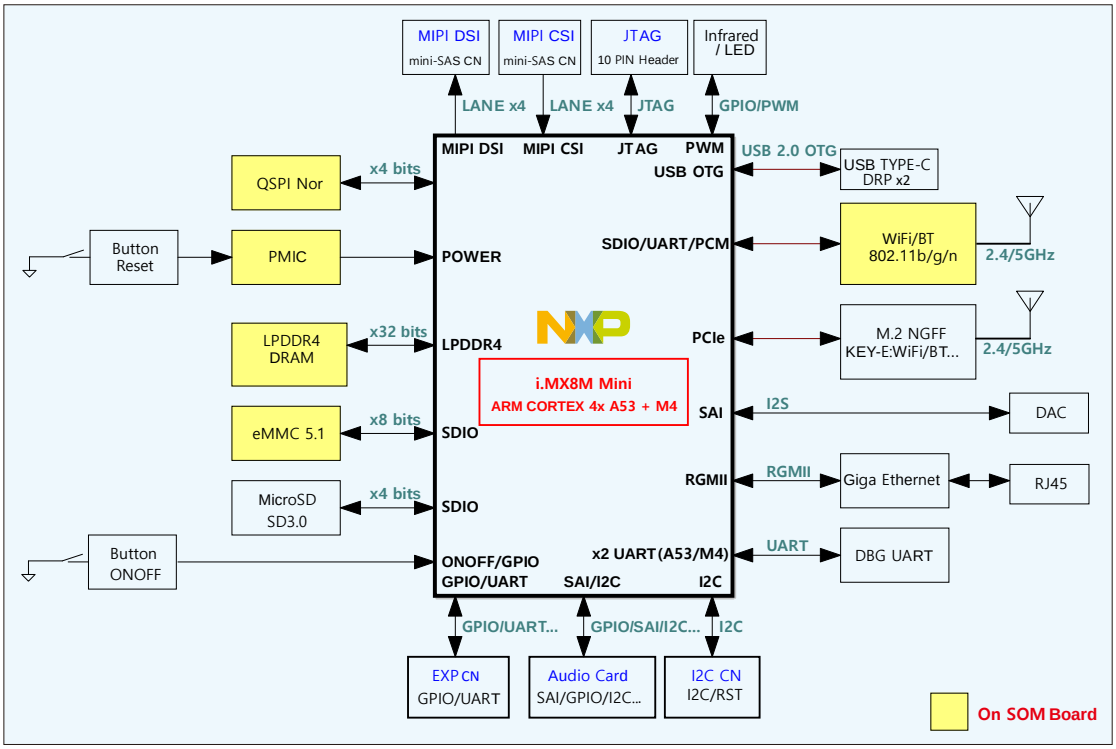
Feature	Specifications
CPU	NXP i.MX8M Mini, 4x Cortex-A53 core platforms @1.8GHz + Cortex-M4 core @ 400MHz
GPU	3D GPU (1x shader, OpenGL® ES 2.0), 2D GPU
Memory	2GB LPDDR4
Flash	8GB eMMC
Power	5V
WiFi&BT	802.11b/g/n WiFi, Bluetooth 4.0
Pin out	UART, USB Host, USB OTG, Gigabit Ethernet, MIPI CSI, MIPI DSI, PCIe, GPIO, SD, JTAG, I2C, SPI, SPDIF, SAI, etc.
Layer	6 layers
Pin number	200 pins
Connector	200-pin SO-DIMM edge connector
Dimension	67.6mm x 34.3 mm

1.4 Block Diagram

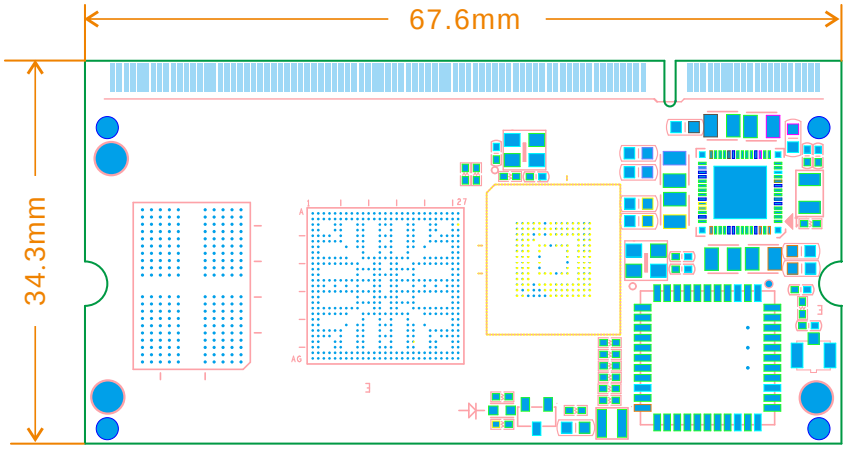
1.4.1 i.MX 8M Mini Block Diagram



1.4.2 Evaluation Kit Block Diagram



1.5 PCB Dimension



1.6 Pin Definition

Pin	Signal	Description	IO Voltage
1	GND	ground	0V
2	GND	ground	0V
3	GND	ground	0V

4	GND	ground	0V
5	GND	ground	0V
6	GND	ground	0V
7	VSYS_5V	System Power 5V input	5V
8	VSYS_5V	System Power 5V input	5V
9	VSYS_5V	System Power 5V input	5V
10	VSYS_5V	System Power 5V input	5V
11	VSYS_5V	System Power 5V input	5V
12	VSYS_5V	System Power 5V input	5V
13	GND	ground	0V
14	GND	ground	0V
15	GND	ground	0V
16	GND	ground	0V
17	NVCC_1V8	1.8V output, Max 500mA	1.8V
18	NVCC_1V8	1.8V output, Max 500mA	1.8V
19	NVCC_1V8	1.8V output, Max 500mA	1.8V
20	NVCC_1V8	1.8V output, Max 500mA	1.8V
21	GND	ground	0V
22	GND	ground	0V
23	NVCC_3V3	3.3V output, Max 1000mA	3.3V
24	NVCC_3V3	3.3V output, Max 1000mA	3.3V
25	NVCC_3V3	3.3V output, Max 1000mA	3.3V
26	M.2_32K_OUT	GPIO1_IO00 or 32.768Khz output	3.3V
27	SAI1_TXD7	GPIO4_IO19/SAI6_MCLK with pull D 4.7K	3.3V
28	SAI1_TXD6	GPIO4_IO18/SAI6_RxSYNC pull Down 10K	3.3V
29	SAI1_TXD5	GPIO4_IO17/SAI6_RxData0 pull Up 10K	3.3V
30	SAI1_TXD4	GPIO4_IO16/SAI6_RxBCLK pull D 4.7K	3.3V
31	SAI1_TXD3	GPIO4_IO15/SAI5_TxData3 pull Up 10K	3.3V
32	SAI1_TXD2	GPIO4_IO14/SAI5_TxData2 pull Down 4.7K	3.3V
33	SAI1_TXD1	GPIO4_IO13/SAI5_TxData1 pull Up 10K	3.3V
34	SAI1_TXD0	GPIO4_IO12/SAI5_TxData0 pull Down 4.7K	3.3V
35	GND	ground	0V
36	SAI1_TXC	GPIO4_IO11/SAI5_TxBCLK	3.3V
37	SAI1_RXC	GPIO4_IO01/SAI5_RxBCLK	3.3V
38	SAI1_TXFS	GPIO4_IO10/SAI5_TxSYNC	3.3V
39	SAI1_RXFS	GPIO4_IO00/SAI5_RxSYNC	3.3V
40	GND	ground	0V
41	SAI1_RXD7	GPIO4_IO09/SAI1_TxSYNC pull D 4.7K	3.3V
42	SAI1_RXD6	GPIO4_IO08/SAI6_TxSYNC pull D 4.7K	3.3V
43	SAI1_RXD5	GPIO4_IO07/SAI6_TxData0 pull Up 10K	3.3V
44	SAI1_RXD4	GPIO4_IO06/SAI6_TxBCK pull D 4.7K	3.3V
45	SAI1_RXD3	GPIO4_IO05/SAI5_RxData3 pull D 4.7K	3.3V
46	SAI1_RXD2	GPIO4_IO04/SAI5_RxData2 pull D 4.7K	3.3V

47	SAI1_RXD1	GPIO4_IO03/SAI5_RxData1 pull Up 10K	3.3V
48	SAI1_RXD0	GPIO4_IO02/SAI5_RxData0 pull Up 10K	3.3V
49	SAI5_RXFS	GPIO3_IO19/SAI1_TxData0	3.3V
50	GND	ground	0V
51	SAI5_RXC	GPIO3_IO20/SAI1_TxData1/PDM_CLK	3.3V
52	SAI5_RXD2	GPIO3_IO23/SAI1_TxSYNC/PDM_Data2	3.3V
53	SAI5_MCLK	GPIO3_IO25/SAI1_TxBCLK	3.3V
54	SAI5_RXD3	GPIO3_IO24/SAI1_TxData5/SAI1_TxSYNC/PDM_Data3	3.3V
55	SAI5_RXD1	GPIO3_IO22/SAI1_TxData3/SAI1_TxSYNC/PDM_Data1	3.3V
56	GND	ground	0V
57	GND	ground	0V
58	SAI5_RXD0	GPIO3_IO21/SAI1_TxData2/PDM_Data0	3.3V
59	PWRON	System reset	1.8V
60	SAI1_MCLK	GPIO4_IO20/SAI5_MCLK/SAI1_TxBCLK/PDM_CLK	3.3V
61	GND	ground	0V
62	GND	ground	0V
63	ENET_TXC	GPIO1_IO23/ENET1_RGMII_TXC/ENET1_TX_ER	3.3V
64	ENET_TX_CTL	GPIO1_IO22/ENET1_RGMII_TX_CTL	3.3V
65	GND	ground	0V
66	ENET_TD0	GPIO1_IO21/ENET1_RGMII_TD0	3.3V
67	ENET_TD1	GPIO1_IO20/ENET1_RGMII_TD1	3.3V
68	ENET_TD2	GPIO1_IO19/ENET1_RGMII_TD2/INPUT=ENET1_TXCLK	3.3V
69	ENET_TD3	GPIO1_IO18/ENET1_RGMII_TD3	3.3V
70	ENET_RX_CTL	GPIO1_IO24/ENET1_RGMII_RX_CTL	3.3V
71	ENET_RXC	GPIO1_IO25/ENET1_RGMII_RXC/ENET1_RX_ER	3.3V
72	GND	ground	0V
73	ENET_RD0	GPIO1_IO26/ENET1_RGMII_RD0	3.3V
74	ENET_RD1	GPIO1_IO27/ENET1_RGMII_RD1	3.3V
75	PMIC_ON_REQ	PMIC require on	1.8V
76	ENET_RD2	GPIO1_IO28/ENET1_RGMII_RD2	3.3V
77	GND	ground	0V
78	ENET_RD3	GPIO1_IO29/ENET1_RGMII_RD3	3.3V
79	USB2_DP	USB2 data positive	3.3V
80	ENET_MDC	GPIO1_IO16/ENET1_MDC	3.3V
81	USB2_DN	USB2 data negative	3.3V
82	ENET_MDIO	GPIO1_IO17/ENET1_MDIO	3.3V
83	GND	ground	0V
84	GND	ground	0V
85	USB1_DP	USB1 data positive	3.3V
86	GND	ground	0V
87	USB1_DN	USB1 data negative	3.3V
88	SD2_CD_B	GPIO2_IO12/usdhc2_CD_B	3.3V
89	GND	ground	0V

90	SD2_WP	GPIO2_IO20/usdhc2_WP	3.3V
91	PCIE_CLK_P	PCIE clock positive	1.8V
92	SD2_CMD	GPIO2_IO14/usdhc2_CMD	3.3V
93	PCIE_CLK_N	PCIE clock negative	1.8V
94	SD2_CLK	GPIO2_IO13/usdhc2_CLK	3.3V
95	GND	ground	0V
96	SD2_RESET_B	GPIO2_IO19/usdhc2_RESET_B	3.3V
97	PCIE_TXN_P	PCIE output positive	1.8V
98	GND	ground	0V
99	PCIE_TXN_N	PCIE output negative	1.8V
100	SD2_DATA0	GPIO2_IO15/usdhc2_DATA0	3.3V
101	GND	ground	0V
102	SD2_DATA1	GPIO2_IO16/usdhc2_DATA1	3.3V
103	PCIE_RXN_P	PCIE input positive	1.8V
104	SD2_DATA2	GPIO2_IO17/usdhc2_DATA2	3.3V
105	PCIE_RXN_N	PCIE input negative	1.8V
106	SD2_DATA3	GPIO2_IO18/usdhc2_DATA3	3.3V
107	GND	GND	0V
108	SD1_STROBE	GPIO2_IO11/usdhc1_STROBE	1.8V
109	MIPI_CSI_D3_P	CSI data3 positive	1.8V
110	BOOT_MODE1	ccmsrcgpcmix_BOOT_MODE1	3.3V
111	MIPI_CSI_D3_N	CSI data3 negative	1.8V
112	BOOT_MODE0	ccmsrcgpcmix_BOOT_MODE0	3.3V
113	GND	ground	0V
114	JTAG_TMS	cjtag_wrapper_TMS	3.3V
115	MIPI_CSI_D2_P	CSI data2 positive	1.8V
116	JTAG_TDO	cjtag_wrapper_TDO	3.3V
117	MIPI_CSI_D2_N	CSI data2 negative	1.8V
118	JTAG_TDI	cjtag_wrapper_TDI	3.3V
119	GND	ground	0V
120	JTAG_TCK	cjtag_wrapper_TCK	3.3V

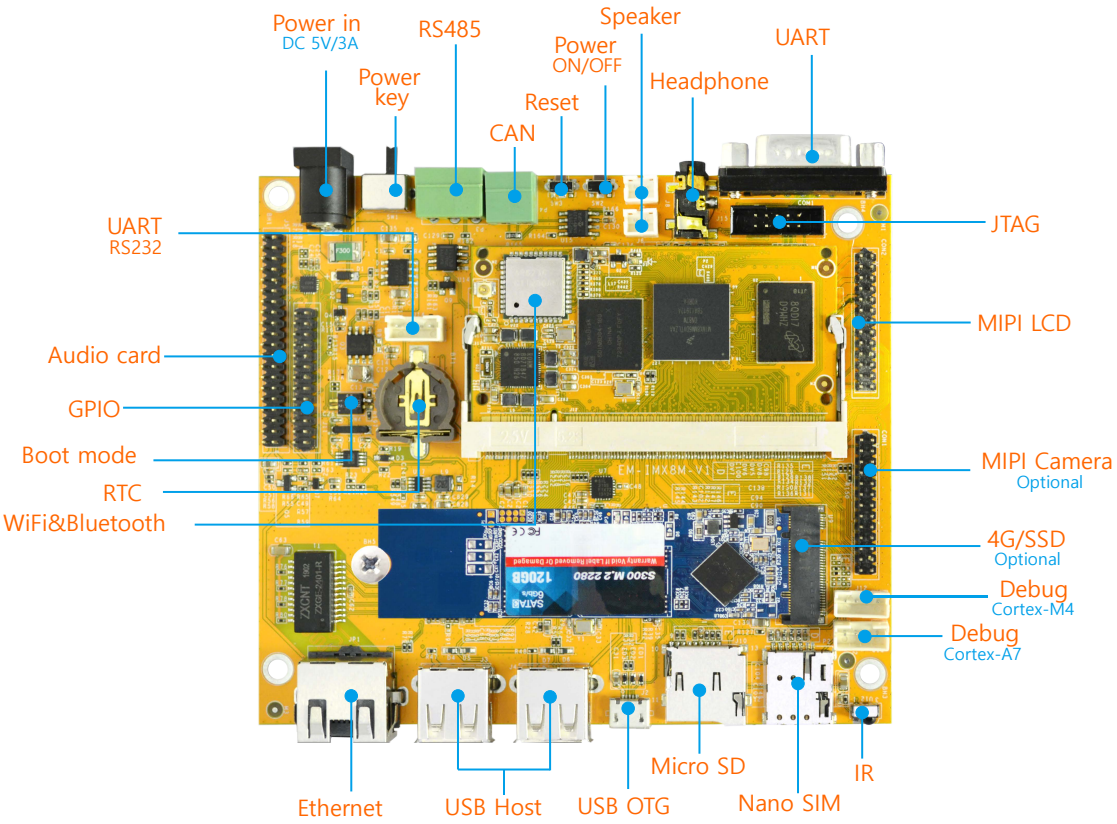
121	MIPI_CSI_CLK_P	CSI clock positive	1.8V
122	JTAG_TRST_B	cjtag_wrapper_TRST_B	3.3V
123	MIPI_CSI_CLK_N	CSI clock negative	1.8V
124	CLKOUT1	anamix_CLKOUT1	1.8V
125	GND	Ground	0V
126	CLKOUT2	anamix_CLKOUT2	1.8V
127	MIPI_CSI_D1_P	CSI data1 positive	1.8.V
128	CLKIN1	anamix_CLKIN1	1.8V
129	MIPI_CSI_D1_N	CSI data1 negative	1.8V
130	CLKIN2	anamix_CLKIN2	1.8V
131	GND	Ground	0V
132	ONOFF	snvsmix_ONOFF	1.8V
133	MIPI_CSI_D0_P	CSI data0 positive	1.8V
134	USB2_VBUS	USB2_VBUS	3.3V
135	MIPI_CSI_D0_N	CSI data0 negative	1.8V
136	USB1_VBUS	USB1_VBUS	3.3V
137	GND	Ground	0V
138	USB2_ID	USB2_ID	3.3V
139	MIPI_DSI_D3_P	DSI data3 positive	1.8V
140	USB1_ID	USB1_ID	3.3V
141	MIPI_DSI_D3_N	DSI data3 negative	1.8V
142	UART4_TXD	GPIO5_IO29/UART2_RTS_B	3.3V

143	GND	Ground	0V
144	UART4_RXD	GPIO5_IO28/UART2_CTS_B/PCIE1_CLKREQ_B	3.3V
145	MIPI_DSI_D2_P	DSI data2 positive	1.8V
146	UART3_TXD	GPIO5_IO27/UART1_RTS_B/usdhc3_VSELECT	3.3V
147	MIPI_DSI_D2_N	DSI data2 negative	1.8V
148	UART3_RXD	GPIO5_IO26/UART1_CTS_B/usdhc3_RESET_B	3.3V
149	GND	Ground	0V
150	UART2_TXD	GPIO5_IO25/ECSPI3_SS0	3.3V
151	MIPI_DSI_CLK_P	DSI clock positive	1.8V
152	UART2_RXD	GPIO5_IO24/ECSPI3_MISO	3.3V
153	MIPI_DSI_CLK_N	DSI clock negative	1.8V
154	UART1_TXD	GPIO5_IO23/ECSPI3_MOSI	3.3V
155	GND	Ground	0V
156	UART1_RXD	GPIO5_IO22/ECSPI3_SCLK	3.3V
157	MIPI_DSI_D1_P	DSI data1 positive	1.8V
158	I2C4_SCL	GPIO5_IO20/PWM2_OUT/PCIE1_CLKREQ_B	3.3V
159	MIPI_DSI_D1_N	DSI data1 negative	1.8V
160	I2C4_SDA	GPIO5_IO21/PWM1_OUT	3.3V
161	GND	ground	0V
162	I2C3_SCL	GPIO5_IO18/PWM4_OUT/gpt2_CLK	3.3V
163	MIPI_DSI_D0_P	DSI data0 positive	1.8V
164	I2C3_SDA	GPIO5_IO19/PWM3_OUT/gpt3_CLK	3.3V

165	MIPI_DSI_D0_N	DSI data0 negative	1.8V
166	I2C2_SCL	GPIO5_IO16/ENET1_1588_EVENT1_IN/usdhc3_CD_B	3.3V
167	GND	Ground	0V
168	I2C2_SDA	GPIO5_IO17/ENET1_1588_EVENT1_OUT/usdhc3_WP	3.3V
169	ECSPI1_SCLK	GPIO5_IO6/UART3_RX	3.3V
170	ECSPI2_MOSI	GPIO5_IO11/UART4_TX	3.3V
171	ECSPI1_MOSI	GPIO5_IO7/UART3_TX	3.3V
172	ECSPI2_MISO	GPIO5_IO12/UART4_CTS_B	3.3V
173	ECSPI1_MISO	GPIO5_IO8/UART3_CTS_B	3.3V
174	ECSPI2_SCLK	GPIO5_IO10/UART4_RX	3.3V
175	ECSPI1_SS0	GPIO5_IO9/UART3_RTS_B	3.3V
176	ECSPI2_SS0	GPIO5_IO13/UART4_RTS_B	3.3V
177	GND	Ground	0V
178	SAI3_TXD	GPIO5_IO1/SAI3_TX_Data0/SAI5_RxData3	3.3V
179	SAI3_TXC	GPIO5_IO0/SAI3_TX_BCLK/SAI5_RxData2/UART2_TX	3.3V
180	SAI3_TXFS	GPIO4_IO31//SAI3_TX_SYNC/SAI5_RxData1/UART2_RX	3.3V
181	SAI3_RXD	GPIO4_IO30/SAI3_RX_Data0/SAI5_RxData0/UART2_RTS_B	3.3V
182	SAI3_MCLK	GPIO5_IO2/PWM4_OUT/SAI5_MCLK	3.3V
183	SAI3_RXC	GPIO4_IO29/SAI3_RX_BCLK/SAI5_RX_BCLK/UART2_CTS_B	3.3V
184	GPIO1_IO13	usb1_OTG_OC/PWM2_OUT	3.3V
185	SAI3_RXFS	GPIO4_IO28/SAI3_RX_SYNC/SAI5_RX_SYNC	3.3V
186	GPIO1_IO10	usb1_OTG_ID	3.3V

187	GPIO1_IO15	usb2_OTG_OC/usdhc3_WP/PWM4_OUT	3.3V
188	GPIO1_IO12	usb1_OTG_PWR/sdma2_EXT_EVENT1	3.3V
189	GPIO1_IO14	usb2_OTG_PWR/usdhc3_CD_B/PWM3_OUT	3.3V
190	GPIO1_IO08	ENET1_1588_EVENT0_IN/usdhc2_RESET_B	3.3V
191	GPIO1_IO05	m4.NMI/ccmsrcgpcmix_PMIC_READY	3.3V
192	GPIO1_IO11	usb2_OTG_ID/usdhc3_VSELECT	3.3V
193	GPIO1_IO07	ENET1_MDIO/usdhc1_WP	3.3V
194	GPIO1_IO01	PWM1_OUT/anamix_REF_CLK_24M	3.3V
195	GPIO1_IO09	ENET1_1588_EVENT0_OUT/usdhc3_RESET_B	3.3V
196	SPDIF_EXT_CLK	GPIO5_IO5/PWM1_OUT	3.3V
197	GPIO1_IO06	ENET1_MDC/usdhc1_CD_B	3.3V
198	SPDIF_RX	GPIO5_IO4/PWM2_OUT	3.3V
199	GND	Ground	0V
200	SPDIF_TX	GPIO5_IO3/PWM3_OUT	3.3V

1.7 Development Kit (EM-IMX8M-MINI)



Feature	Specifications
CPU	i.MX 8MQuad, 4x ARM Cortex-A53 @ 1.8 GHz +ARM Cortex-M4 @ 400 MHz
GPU	OpenGL ES1.1,2.0, OpenVG1.1
Memory	2GB LPDDR4
Storage	8GB eMMC flash
Power Management	ROHM BD71847
Power Input	DC 5V/3A
USB	1x USB 2.0 OTG, 2x USB 2.0 Host
UART	1x RS232(COM1), 3x UARTs (J12, J13, J14)
Ethernet	Gigabit Ethernet port, RJ45 connector. Realtek RTL8211E
Audio	WM8960 audio codec. 3.5mm audio jack, 2x 2pin header for Speaker
Expand Audio	8bit RX and 8bit TX SAI interface, 40-pin header (J5)
SD	Micro SD socket, SD3.01
Display	MIPI-DSI, 4 data lanes, up to 1920 x 1080 @60Hz, 26-pin header (CON2)
RTC	Real time clock, powered by external battery
JTAG	JTAG debug interface, 10-pin header
CAN	2-Pin connector (P4)

RS485	Compatible 9-bit data format, 3-pin connector (P3)
Buttons	Reset (SW2), Power (SW3), Boot Mode (SW4)
Expand interface	2x I2C, 1x SPI, 6x GPIO, 26-pin header (J11)
PCIe	Support USB2.0, PCIE2.1, UIM interface for SSD or 4G module
Camera	MIPI-CSI, 4 data lanes, 26-pin header (CON1)
WiFi&Bluetooth	802.11b/g/n WiFi, Bluetooth 4.0. AP6236 chipset
SIM	Nano SIM
Dimension	102.3mm x 118.6mm

2 Peripheral Introduction

Some pins are multifunctional. Pin function selection is controlled by software. Each pin can be used for a single function at a time.

eg. **SAI1_RXFS**

The default pin is Pin39, and Pin43 (default function SAI1_RXD5) also can be used for ***SAI1_RXFS****.*

2.1 Display

MIPI DSI Features

- 4- lane MIPI-DSI up to 1920 x 1080 @ 60Hz
- Touchscreen capacitive touch-screen support through I2C interfaces
- Up to a maximum bit rate of 1.5 Gbps.

Signal	Description	Pin	Defaults Function
DSI_DP0	MIPI-DSI data0 diff-pair Positive	163	DSI_DP0
DSI_DN0	MIPI-DSI data0 diff-pair Negative	165	DSI_DN0
DSI_DP1	MIPI-DSI data1 diff-pair Positive	157	DSI_DP1
DSI_DN1	MIPI-DSI data1 diff-pair Negative	159	DSI_DN1
DSI_DP2	MIPI-DSI data2 diff-pair Positive	145	DSI_DP2
DSI_DN2	MIPI-DSI data2 diff-pair Negative	147	DSI_DN2
DSI_DP3	MIPI-DSI data3 diff-pair Positive	139	DSI_DP3
DSI_DN3	MIPI-DSI data3 diff-pair Negative	141	DSI_DN3
DSI_CKP	MIPI-DSI clock diff-pair Positive	151	DSI_CKP
DSI_CKN	MIPI-DSI clock diff-pair Negative	153	DSI_CKN

2.2 Camera I/F

- Configurable interface logic to support most commonly available CMOS sensors

- Support up to 4 data lanes
- Support 80Mbps - 1.5Gbps data rate in high speed operation

MIPI CSI signals

Signal	Description	Pin	Defaults Function
CSI_DP0	MIPI-CSI data0 diff-pair Positive	133	CSI_DP0
CSI_DN0	MIPI-CSI data0 diff-pair Negative	135	CSI_DN0
CSI_DP1	MIPI-CSI data1 diff-pair Positive	127	CSI_DP1
CSI_DN1	MIPI-CSI data1 diff-pair Negative	129	CSI_DN1
CSI_DP2	MIPI-CSI data2 diff-pair Positive	115	CSI_DP2
CSI_DN2	MIPI-CSI data2 diff-pair Negative	117	CSI_DN2
CSI_DP3	MIPI-CSI data3 diff-pair Positive	109	CSI_DP3
CSI_DN3	MIPI-CSI data3 diff-pair Negative	111	CSI_DN3
CSI_CKP	MIPI-CSI clock diff-pair Positive	121	CSI_CKP
CSI_CKN	MIPI-CSI clock diff-pair Negative	123	CSI_CKN

2.3 Audio

2.3.1 Digital Interface (SAI)

Five synchronous audio interface (SAI) modules supporting I2S, AC97, TDM, codec/DSP, and DSD interfaces, including one SAI with 8 Tx and 8 Rx lanes, one SAI with 4 Tx and 4 Rx lanes, two SAI with 2 Tx and 2 Rx lanes, and one SAI with 1 Tx and 1Rx lane. Support over 20 channels of audio subject to I/O limitations. 8-Channel Pulse Density Modulation (PDM) input.

Signal	Description	Pin	Defaults Function
SAI1_RXD0	SAI1 Receive data0	48	SAI1_RXD0
SAI1_RXD1	SAI1 Receive data1	47	SAI1_RXD1
SAI1_RXD2	SAI1 Receive data2	46	SAI1_RXD2
SAI1_RXD3	SAI1 Receive data3	45	SAI1_RXD3
SAI1_RXD4	SAI1 Receive data4	44	SAI1_RXD4
SAI1_RXD5	SAI1 Receive data5	43	SAI1_RXD5
SAI1_RXD6	SAI1 Receive data6	42	SAI1_RXD6
SAI1_RXD7	SAI1 Receive data7	41	SAI1_RXD7
SAI1_RXC	SAI1 Receive bit clock	37	SAI1_RXC
SAI1_RXFS	Receive frame sync	39	SAI1_RXFS
		43	SAI1_RXD5
SAI1_TXD0	SAI1 Transmit data0	34	SAI1_TXD0
		49	SAI5_RXFS
SAI1_TXD1	SAI1 Transmit data1	33	SAI1_TXD1
		51	PDM_CLK
SAI1_TXD2	SAI1 Transmit data2	32	SAI1_TXD2
		58	PDM_DATA0

SAI1_TXD3	SAI1 Transmit data3	31	SAI1_TXD3
		55	PDM_DATA1
SAI1_TXD4	SAI1 Transmit data4	30	SAI1_TXD4
		52	PDM_DATA2
		41	SAI1_RXD7
SAI1_TXD5	SAI1 Transmit data5	29	SAI1_TXD5
		52	PDM_DATA3
SAI1_TXD6	SAI1 Transmit data6	28	SAI1_TXD6
SAI1_TXD7	SAI1 Transmit data7	27	SAI1_TXD7
SAI1_TXC	SAI1 Transmit bit clock	36	SAI1_TXC
		53	SAI5_MCLK
		60	SAI1_MCLK
SAI1_TXFS	SAI1 Transmit frame sync	38	SAI1_TXFS
		55	PDM_DATA1
SAI1_MCLK	SAI1 Main Clock	60	SAI1_MCLK
		52	PDM_DATA2
		54	PDM_DATA3
		41	SAI1_RXD7
SAI3_RXD	SAI3 Receive data	181	SAI3_RXD
SAI3_RXC	SAI3 Receive bit clock	183	SAI3_RXC
SAI3_RXFS	SAI3 Receive frame sync	185	SAI3_RXFS
SAI3_TXD	SAI3 Transmit data	178	SAI3_TXD
SAI3_TXC	SAI3 Transmit bit clock	179	SAI3_TXC
SAI3_TXFS	SAI3 Transmit frame sync	180	SAI3_TXFS
SAI3_MCLK	SAI3 main clock	182	SAI3_MCLK
SAI5_RXD0	SAI5 Receive data0	58	PDM_DATA0
		48	SAI1_RXD0
		181	SAI3_RXD
SAI5_RXD1	SAI5 Receive data1	55	PDM_DATA1
		47	SAI1_RXD1
		180	SAI3_TXFS
SAI5_RXD2	SAI5 Receive data2	52	PDM_DATA2
		46	SAI1_RXD2
		179	SAI3_TXC
SAI5_RXD3	SAI5 Receive data3	54	PDM_DATA3
		45	SAI1_RXD3
		178	SAI3_TXD
SAI5_RXC	SAI5 Receive bit clock	51	PDM_CLK
		37	SAI1_RXC
		183	SAI3_RXC
SAI5_RXFS	SAI5 Receive frame sync	49	SAI5_RXFS
		39	SAI1_RXFS
		185	SAI3_RXFS

SAI5_TXD0	SAI5 Transmit data0	34	SAI1_TXD0
		54	PDM_DATA3
SAI5_TXD1	SAI5 Transmit data1	33	SAI1_TXD1
SAI5_TXD2	SAI5 Transmit data2	32	SAI1_TXD2
SAI5_TXD3	SAI5 Transmit data3	31	SAI1_TXD3
SAI5_TXC	SAI5 Transmit bit clock	36	SAI1_TXC
		52	PDM_DATA2
SAI5_TXFS	SAI5 Transmit frame sync	38	SAI1_TXFS
		55	PDM_DATA1
SAI5_MCLK	SAI5 main clock	53	SAI5_MCLK
		60	SAI1_MCLK
		182	SAI3_MCLK

2.3.2 Sony/Philips Digital Interface

S/PDIF input and output, including a new Raw Capture input mode.

Signal	Description	Pin	Defaults Function
SPDIF_RX	SPDIF input data	198	SPDIF_RX
SPDIF_TX	SPDIF output data	200	SPDIF_TX
SPDIF_EXT_CLK	External clock signal	196	SPDIF_EXT_CLK

2.4 Ethernet

The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. Used PHY chip RTL8211E-VB-CG,

Features

- 1000Base-T IEEE 802.3ab Compliant
- 1000Base-TX IEEE 802.3u Compliant
- Supports RGMII
- Crossover Detection & Auto-Correction

Signal	Description	Pin	Defaults Function
ENET_RD0	Ethernet MAC Receive data0	73	ENET_RD0
ENET_RD1	Ethernet MAC Receive data1	74	ENET_RD1
ENET_RD2	Ethernet MAC Receive data2	76	ENET_RD2
ENET_RD3	Ethernet MAC Receive data3	78	ENET_RD3
ENET_RXC	Ethernet MAC Receive clock	71	ENET_RXC
ENET_RX_CTL	Ethernet MAC Receive enable control	70	ENET_RX_CTL
ENET_TD0	Ethernet MAC Transmit data0	66	ENET_TD0
ENET_TD1	Ethernet MAC Transmit data1	67	ENET_TD1
ENET_TD2	Ethernet MAC Transmit data2	68	ENET_TD2
ENET_TD3	Ethernet MAC Transmit data3	69	ENET_TD3
ENET_TXC	Ethernet MAC Transmit clock	63	ENET_TXC

ENET_TX_CTL	Ethernet MAC Transmit enable control	64	ENET_TX_CTL
ENET_MDC	MAC and PHY Communication clock	80	ENET_MDC
ENET_MDIO	MAC and PHY Communication data	82	ENET_MDIO
ENET_nINT	ENET interrupt	186	GPIO1_IO10

2.5 USB

Two USB controllers and PHYs that support USB 2.0 and OTG. Each USB instance contains USB 2.0 core, which can operate in 2.0 mode.

Signal	Description	Pin	Defaults Function
USB1_DP	USB1 positive data	85	USB1_DP
USB1_DN	USB1 negative data	87	USB1_DN
USB1_ID	USB1 OTG ID signal	140	USB1_ID
USB1_VBUS_DET	USB1 VBUS detect	136	USB1_VBUS_DET
USB2_DP	USB2 positive data	79	USB2_DP
USB2_DN	USB2 negative data	81	USB2_DN
USB2_ID	USB2 OTG ID signal	138	USB2_ID
USB2_VBUS_DET	USB1 VBUS detect	134	USB2_VBUS_DET

2.6 PCIe

PCI-E Features:

- Single lane supporting PCIe Gen2
- Dual mode operation to function as root complex or endpoint
- Integrated PHY interface
- Support L1 low power sub-state

Signal	Description	Pin	Defaults Function
PCIE_RXP	PCIE receive data positive	103	PCIE_RXP
PCIE_RXN	PCIE receive data negative	105	PCIE_RXN
PCIE_TXP	PCIE transmit data positive	97	PCIE_TXP
PCIE_TXN	PCIE transmit data positive	99	PCIE_TXN
PCIE_CLKP	PCIe reference clock dif input positive	91	PCIE_CLKP
PCIE_CLKN	PCIe reference clock dif input negative	93	PCIE_CLKN

2.7 EMMC/SD/SDIO

2.7.1 EMMC 5.1

- Fully compliant with MMC v5.1/v5.0/v4.4/v4.41/v4.4/v4.3/v4.2
- Support 1bit,4bit(ddr), 8bit(ddr) mode,
- Up to HS400 speed mode

Signal	Description	Pin	Defaults Function
SD3_DATA0	SDIO3 data0	Un-pinout	SD3_DATA0 for emmc
SD3_DATA1	SDIO3 data1	Un-pinout	SD3_DATA1 for emmc
SD3_DATA2	SDIO3 data2	Un-pinout	SD3_DATA2 for emmc
SD3_DATA3	SDIO3 data3	Un-pinout	SD3_DATA3 for emmc
SD3_DATA4	SDIO3 data4	Un-pinout	SD3_DATA4 for emmc
SD3_DATA5	SDIO3 data5	Un-pinout	SD3_DATA5 for emmc
SD3_DATA6	SDIO3 data6	Un-pinout	SD3_DATA6 for emmc
SD3_DATA7	SDIO3 data7	Un-pinout	SD3_DATA7 for emmc
SD3_CMD	SDIO3 Command	Un-pinout	SD3_CMD for emmc
SD3_CLK	SDIO3 Clock	Un-pinout	SD3_CLK for emmc

2.7.2 SD/SDIO3.0

SD/SDIO 3.0 compliance with 200 MHz SDR signaling to support up to 100 MB/sec

Support for SDXC (extended capacity)

SD card signals

Signal	Description	Pin	Defaults Function
SD2_DATA0	SDIO2 data0	100	SD2_DATA0
SD2_DATA1	SDIO2 data1	102	SD2_DATA1
SD2_DATA2	SDIO2 data2	104	SD2_DATA2
SD2_DATA3	SDIO2 data3	106	SD2_DATA3
SD2_nCD	SDIO2 Detect	88	SD2_nCD
SD2_WP	SDIO2 Write Protect	90	SD2_WP
SD2_nRST	SDIO2 Reset	96	SD2_nRST
SD2_CMD	SDIO2 Command	92	SD2_CMD
SD2_CLK	SDIO2 Clock	94	SD2_CLK

SDIO Wireless signal

Signal	Description	Pin	Defaults Function
SD1_DATA0	SDIO1 data0	Un-pinout	SD1_DATA0 for wifi
SD1_DATA1	SDIO1 data1	Un-pinout	SD1_DATA1 for wifi
SD1_DATA2	SDIO1 data2	Un-pinout	SD1_DATA2 for wifi
SD1_DATA3	SDIO1 data3	Un-pinout	SD1_DATA3 for wifi
SD1_DATA4	SDIO1 data4	Un-pinout	BT_REG_ON for wifi
SD1_DATA5	SDIO1 data5	Un-pinout	BT_WAKE_DEV for wifi
SD1_DATA6	SDIO1 data6	Un-pinout	BT_WAKE_HOST for wifi
SD1_DATA7	SDIO1 data7	Un-pinout	WL_WAKE_HOST for wifi
SD1_CMD	SDIO1 Command	Un-pinout	SD1_CMD for wifi
SD1_CLK	SDIO1 Clock	Un-pinout	SD1_CLK for wifi

2.8 SPI

2.8.1 ECSPI

Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. Configurable to support Master/Slave modes, four chip selects to support multiple peripherals.

Signal	Description	Pin	Defaults Function
ECSPI1_SCLK	SPI1 Master clock put out;	169	UART3_RXD
ECSPI1_MISO	SPI1 Master data input; Slave data output	173	UART3_CTS
ECSPI1_MOSI	SPI1 Slave data input; Master data output	171	UART3_TXD
ECSPI1_SS0	SPI1 Chip Select0	175	UART3_RTS
ECSPI2_SCLK	SPI2 Master clock put out;	174	ECSPI2_SCLK
ECSPI2_MISO	SPI2 Master data input; Slave data output	172	ECSPI2_MISO
ECSPI2_MOSI	SPI2 Slave data input; Master data output	170	ECSPI2_MOSI
ECSPI2_SS0	SPI2 Chip Select0	176	ECSPI2_SS0
ECSPI3_SCLK	SPI3 Master clock put out;	156	UART1_RXD
ECSPI3_MISO	SPI3 Master data input; Slave data output	154	UART1_TXD
ECSPI3_MOSI	SPI3 Slave data input; Master data output	152	UART2_RXD
ECSPI3_SS0	SPI3 Chip Select0	150	UART2_TXD

2.8.2 QSPI

Signal	Description	Pin	Defaults Function
QSPIA_SCLK	SPIA Master clock put out;	Un-pinout	QSPIA_SCLK for flash
QSPIA_SS0	SPIA Chip Select0	Un-pinout	QSPIA_SS0 for flash
QSPIA_SS1	SPIA Chip Select1	Un-pinout	SD3_STROBE for emmc
QSPIA_data0	SPIA data0	Un-pinout	QSPIA_data0 for flash
QSPIA_ data1	SPIA data1	Un-pinout	QSPIA_ data1 for flash
QSPIA_ data2	SPIA data2	Un-pinout	QSPIA_ data2 for flash
QSPIA_ data3	SPIA data3	Un-pinout	QSPIA_ data3 for flash
QSPIB_SCLK	SPIB Master clock put out;	Un-pinout	SD3_DATA7 for emmc
QSPIB_SS0	SPIB Chip Select0	Un-pinout	SD3_DATA5 for emmc
QSPIB_SS1	SPIB Chip Select1	Un-pinout	SD3_DATA6 for emmc
QSPIB_data0	SPIB data0	Un-pinout	SD3_DATA0 for emmc
QSPIB_ data1	SPIB data1	Un-pinout	SD3_DATA1 for emmc
QSPIB_ data2	SPIB data2	Un-pinout	SD3_DATA2 for emmc
QSPIB_ data3	SPIB data3	Un-pinout	SD3_DATA3 for emmc

2.9 UART

Four Universal Asynchronous Receiver/Transmitter (UART) modules

Each of the UARTv2 modules supports the following serial data transmit/receive protocols and

configurations:

- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd, or none)
- Programmable baud rates up to 4 Mbps. This is a higher max baud rate relative to the 1.875 MHz, which is stated by the TIA/EIA-232-F standard.
- 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud

Signal	Description	Pin	Defaults Function
UART1_CTS_B	UART1 clear to send	16	UART3_RXD
UART1_RTS_B	UART1 request to send	171	UART3_TXD
UART1_RXD	UART1 data input	156	UART1_RXD
UART1_TXD	UART1 data output	154	UART1_TXD
UART2_CTS_B	UART2 clear to send	144	UART4_RXD
		182	SAI3_RXC
UART2_RTS_B	UART2 request to send	142	UART4_TXD
		181	SAI3_RXD
UART2_RXD	UART2 data input	152	UART2_RXD
		185	SAI3_TXFS
UART2_TXD	UART2 data output	150	UART2_TXD
		179	SAI3_TXC
UART3_CTS_B	UART3 clear to send	173	UART3_CTS_B
UART3_RTS_B	UART3 request to send	175	UART3_RTS_B
UART3_RXD	UART3 data input	169	UART3_RXD
		148	UART1_CTS
UART3_TXD	UART3 data output	171	UART3_TXD
		146	UART1_RTS
UART4_CTS_B	UART4 clear to send	172	ECSPI2_MISO
UART4_RTS_B	UART4 request to send	176	ECSPI2_SS0
UART4_RXD	UART4 data input	144	UART4_RXD
		174	ECSPI2_SCLK
UART4_TXD	UART4 data output	142	UART4_RXD
		170	ECSPI2_MOSI

2.10 I2C

The Inter-Integrated Circuit (I2C) provides functionality of a standard I2C master and slave. The I2C is designed to be compatible with the I2C Bus Specification, version 2.1, by Philips Semiconductor.
I2C provides serial interface for external devices. Data rates of up to 320 kbps are supported.

Signal	Description	Pin	Defaults Function
I2C1_SCL	I2C1 serial clock	Un-pinout	Communication t0 PMIC
I2C1_SDA	I2C1 serial data	Un-pinout	Communication t0 PMIC
I2C2_SCL	I2C2 serial clock	166	I2C2_SCL
I2C2_SDA	I2C2 serial data	168	I2C2_SDA

I2C3_SCL	I2C3 serial clock	162	I2C3_SCL
I2C3_SDA	I2C3 serial data	164	I2C3_SDA
I2C4_SCL	I2C4 serial clock	158	I2C4_SCL
I2C4_SDA	I2C4 serial data	160	I2C4_SDA

2.11 PWM

The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.

Signal	Description	Pin	Defaults Function
PWM1	PWM1 output	194	GPIO1_IO01
		196	SPDIF_EXT_CLK
		160	I2C4_SDA
PWM2	PWM2 output	184	GPIO1_IO13
		198	SPDIF_RX
		158	I2C4_SCL
PWM3	PWM3 output	189	GPIO1_IO14
		200	SPDIF_TX
		164	I2C3_SDA
PWM4	PWM4 output	187	GPIO1_IO15
		182	SAI3_MCLK
		162	I2C3_SCL

2.12 JTAG

Support for 6-pin (JTAG) debug interface

Signal	Description	Pin	Defaults Function
JTAG MOD	JTAG MODE	Un-pinout	
JTAG nTRST	JTAG reset	122	JTAG nTRST
JTAG TCK	JTAG clock	120	JTAG TCK
JTAG TDI	JTAG data input	118	JTAG TDI
JTAG TDO	JTAG data output	116	JTAG TDO
JTAG TMS	JTAG mode select	114	JTAG TMS

3 Product Electrical Characteristics

3.1 Dissipation and Temperature

Symbol	Parameter	Min	Typ	Max	Unit
VSYS	System Voltage	3.8	5	6	V
VCC_IO	System IO Voltage	3.3-5%	3.3	3.3+5%	V
Isys_in	VSYS input Current		800	1500	mA
Ivio_out	VCC_IO output Current		1000	1200	mA
VCC_RTC	RTC Voltage	1.8	3	3.4	V
Iirtc	RTC input Current		5	7	uA
Ta	Operating Temperature	0		70	°C
Tstg	Storage Temperature	-20		85	°C

3.2 Reliability of Test

High Temperature Operating Test		
Contents	Operating 8h in high temperature	55°C±2°C
Result	Pass	

Operating Life Test		
Contents	Operating in room	120h
Result	Pass	