Rockchip RV1108 Datasheet

Revision 1.5
Nov. 2019

Revision History

Date	Revision	Description
2019-11-7	1.5	Update the mark information
2018-6-11	1.4	Add RV1108K1
2017-8-14	1.3	Update ball map information
2017-4-1	1.2	Update IO information
2017-3-20	1.1	Update
2017-1-10	1.0	Initial Release

Table of Content

Figure Index

Table Index

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Chapter 1 Introduction

RV1108 is a high performance low power application processor. It is embedded with a new generation DSP for digital process and an ARM Cortex-A7 single core processor for system and application. Especially, it is a high-integration and cost efficient SoC which can support H.264 video encoder/decoder up to 1440p, up to 4 camera inputs simultaneously, merge different camera sources together and display on one screen.

It is designed for varies application scenario such as car DVR, sports DV, secure camera and UAV camera.
RV1108 support lots of camera interface such as MIPI-CSI, CVBS in and 12-bit parallel raw and it also support lots of display interface such as MIPI-DSI, HDMI 1.4, CVBS out and serial/parallel RGB.

RV1108G package with 16bit DDR3 chip to meet a high-performance up to 800MHz and make cost lower.

1.1 Features

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

1.1.1 Microprocessor

- Single-core ARM Cortex-A7 Core processor, a high-performance, low-power and cached application processor
- Full implementation of the ARM architecture v7-A instruction set, ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation
- Separately integrated NEON and FPU
- 32KB/32KB L1 I-Cache/D-Cache
- Unified 128KB L2 Cache.
- Trustzone technology support

1.1.2 Video/Image Digital Signal Processor

- 32KB I-TCM and 32KB I-cache
- 128KB D-TCM

1.1.3 Memory Organization

- Internal on-chip memory
  - BootRom
  - Internal SRAM
- External off-chip memory①
  - DDR3/DDR3L
  - Async NAND Flash

1.1.4 Internal Memory

- Internal BootRom
  - Size : 10KB
  - Support system boot from the following device :
    - 8bits Async NAND Flash
    - SPI interface
    - eMMC interface
    - SDMMC interface
  - Support system code download by the following interface:
    - USB OTG interface

- Internal SRAM
  - Size : 12KB

1.1.5 External Memory or Storage device

- Dynamic Memory Interface (DDR3/DDR3L)
  - Compatible with JEDEC standard DDR3-1600/DDR3L-1600 SDRAM
  - Supports 16 Bits data width, 1 ranks (chip selects), totally 512MB (max) address space.
  - Programmable timing parameters to support DDR3/DDR3L SDRAM from various vendor
  - Advanced command reordering and scheduling to maximize bus utilization
  - Low power modes, such as power-down and self-refresh for DDR3 SDRAM; Compensation for board delays and variable latencies through programmable pipelines
  - Programmable output and ODT impedance with dynamic PVT compensation

- NAND Flash Interface
  - Support 8bits async NAND flash
  - 16bits hardware ECC
  - For async NAND flash, support configurable interface timing,
  - maximum data rate is 8bit/cycle
  - Embedded AHB master interface to do data transfer by DMA method

- eMMC Interface
  - Compatible with standard iNAND interface
  - Support MMC4.51 protocol
  - Provide eMMC boot sequence to receive boot data from external eMMC device
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Embedded clock frequency division control to provide programmable baud rate
  - Support block size from 1 to 65535Bytes
  - 8bits data bus width

- SD/MMC Interface
  - Compatible with SD3.0, MMC ver4.51
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Support block size from 1 to 65535Bytes
  - Data bus width is 4bits

1.1.6 System Component

- CRU (clock & reset unit)
  - Support clock gating control for individual components inside RV1108
  - One oscillator with 24MHz clock input and 3 embedded PLLs
  - Support global soft-reset control for whole SOC, also individual soft-reset for every components

- Timer
  - 2 on-chip 64bits Timers in SoC with interrupt-based operation
  - Provide two operation modes: free-running and user-defined count
  - Support timer work state checkable
  - Fixed 24MHz clock input

- PWM

- Eight on-chip PWMs with interrupt-based operation
- Programmable pre-scaled operation to bus clock and then further scaled
- Embedded 32-bit timer/counter facility
- Support capture mode
- Support continuous mode or one-shot mode
- Provides reference mode and output various duty-cycle waveform

- WatchDog
  - 32 bits watchdog counter width
  - Counter clock is from APB bus clock
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Programmable reset pulse length
  - Totally 16 defined-ranges of main timeout period

- Bus Architecture
  - 128bit/64-bit/32-bit multi-layer AXI/AHB/APB composite bus architecture
  - 5 embedded AXI interconnect
    - CPU interconnect with one 128-bits AXI masters, one APB slaves
    - DSP interconnect with two 128-bits AXI masters, one 128-bits AXI slave, one 32-bits APB master and many 32-bits APB slaves
    - PERI interconnect with eight 32-bits AHB masters and lots of 32-bits AHB/APB slaves
    - Display interconnect with two 128-bits AXI master, seven 64-bits AXI masters and lots 32-bits AHB/APB slave
    - VENC interconnect with two 128-bits AXI masters, and one 32-bits AHB slaves
    - VDEC interconnect also with two 64-bits AXI master and two 32-bits AHB slaves
  - Flexible different QoS solution to improve the utility of bus bandwidth

- Interrupt Controller
  - Support 3 PPI interrupt source and 128 SPI interrupt sources input from different components inside RV1108
  - Support 16 software-triggered interrupts
  - Input interrupt level is fixed , only high-level sensitive
  - Two interrupt outputs (nFIQ and nIRQ)separately for each Cortex-A7, both are low-level sensitive
  - Support different interrupt priority for each interrupt source, and they are always software-programmable
  - One non-maskable interrupt for DSP
  - Four hardware maskable interrupts for DSP
  - Four software maskable interrupts

- DMAC
  - Micro-code programming based DMA
  - The specific instruction set provides flexibility for programming DMA transfers
  - Linked list DMA function is supported to complete scatter-gather transfer
  - Support internal instruction cache
  - Embedded DMA manager thread
  - Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
  - Signals the occurrence of various DMA events using the interrupt output signals
  - Mapping relationship between each channel and different interrupt outputs is software-programmable
  - One embedded DMA controller for system

- DMAC features:
  - 8 channels totally
  - 16 hardware request from peripherals
  - 2 interrupt output
  - Dual APB slave interface for register configuration, designated as secure and non-secure
  - Support trustzone technology and programmable secure state for each DMA channel

- Security system
  - Embedded encryption and decryption engine
    - Support AES 128/192/256 bits key mode, ECB/CBC/CTR chain mode, Slave/FIFO mode
    - Support DES/3DES (ECB and CBC chain mode) , 3DES (EDE/ EEE key mode), Slave/FIFO mode
    - Support SHA1/SHA256/MD5 (with hardware padding) HASH function, FIFO mode only
    - Support 160 bit Pseudo Random Number Generator (PRNG)
    - Support PKA 512/1024/2048 bit Exp Modulator

1.1.7 Camera interface

- ISP
  - Generic Sensor Interface with programmable polarity for synchronization signals
  - ITU-R BT 601/656 compliant video interface supporting YCbCr or RGB Bayer data
  - 12 bit camera interface
  - 12 bit resolution per color component internally
  - YCbCr 4:2:2 processing
  - Flash light control
  - Mechanical shutter support
  - Windowing and frame synchronization
  - Frame skip support for video (e.g. MPEG-4) encoding
  - Macro block line, frame end, capture error, data loss interrupts and sync. (h_start, v_start) interrupts
  - Luminance/chrominance and chrominance blue/red swapping for YUV input signals
  - Continuous resize support
  - Buffer in system memory organized as ring-buffer
  - Buffer overflow protection for raw data
  - Asynchronous reset input, software reset for the entire IP and separate software resets for all sub-modules
  - Interconnect test support
  - Semi planar storage format
  - Color processing (contrast, saturation, brightness, hue, offset, range)
  - Power management by software controlled clock disabling of currently not needed sub-modules
  - Read port provided to read back a picture from system memory
  - Black level compensation
  - Four channel Lens shade correction (Vignetting)
  - Auto focus measurement
  - White balancing and black level measurement
  - Auto exposure support by brightness measurement in 5x5 sub windows
  - Defect pixel cluster correction unit (DPCC) supports on the fly and table based pixel correction
  - De-noising pre filter (DPF)
  - Enhanced color interpolation (RGB Bayer demosaic)
  - Chromatic aberration correction
  - Combined edge sensitive Sharpening / Blurring filter (Noise filter)

- Color correction matrix (cross talk matrix)
- Image Stabilization support and Video Stabilization Measurement
- Flexible Histogram calculation
- Digital image effects (Emboss, Sketch, Sepia, B/W (Grayscale), Color Selection, Negative image, sharpening)
- Solarize effect through gamma correction
- AXI 64 bit interface 32Bit Address range (two DMA-write ports and one DMA-read port)
- Up to 16 Beat Bursts depending on configured FIFO size
- 32 bit AHB programming interface
- Maximum input resolution of 3264x2448 pixels
- Main scaler with pixel-accurate up- and down-scaling to any resolution between 3264x2448 and 32x16 pixel in processing mode
- Self scaler with pixel-accurate up- and down-scaling to any resolution between 1920x1080 and 32x16 pixel in processing mode
- Support of semiplanar NV21 color storage format
- Support of image cropping
- Support Y12BIT and UV 8BIT path output after GAMMAOUT module
- Support RGB output after GAMMAOUT module
- Support hurry for latency FIFO
- Support Two-in-one RK-Tone-Mapping with wide dynamic range unit (Block/Global WDR)
- Support Video Stabilization Measurement (VSM) Programming update to 3264x2448

- CIF
  - Support YCbCr422 input
  - Support Raw 8bit input
  - Support CCIR656(PAL/NTSC) input
  - Support 1/2/4 channels mixed data of CCIR656 input
  - Support JPEG input
  - Support YCbCr422/420 output
  - Support UYVY/VYUY/YUYV/YVYU configurable
  - Support up to 8192x8192 resolution source
  - Support picture in picture
  - Support arbitrary size window crop
  - Support error/terminate interrupt and combined interrupt output
  - Support CLK/VSYNC/HREF polarity configurable
  - Support one frame stop/ping-pong mode

- TV DECODER
  - Support formats
    - PAL
    - NTSC
    - NTSC or PAL standard is automatically selected depending on the detected input line standard
  - Support auto gain control

- VADC
  - Sample frequency up to 54MHz
  - Support 2’s complement 10bit output
  - The gain of programmable amplifier can be adjusted from 0.5 to 2
  - Support internal buffer circuit

- Support low pass filter

1.1.8 Video CODEC

- Video Decoder
  - Real-time video decoder of H.264
  - Supports frame timeout interrupt , frame finish interrupt and bit stream error interrupt
  - Error detection and concealment support for all video formats
  - Output data format YUV420 semi-planar,YUV400(monochrome) ,YUV422 is supported by H.264
  - H.264 8bit up to HP level 5.0 : 1440p@30fps (2560x1440)

- Video Encoder
  - Support video encoder for H.264 UP to HP@level4.2
  - Only support I and P slices ,not B slices
  - Support CBR and VBR
  - Support 8-area OSD insertion
  - Support Link table configuration for high frame rate application
  - Support ROI
  - Support Slice split
  - Support Low latency encoding
  - Support Color domain conversion
  - Support Cropping and mirror
  - Support De-noise and enhancement
  - Input data format:
    - YCbCr 4:2:0 planar
    - YCbCr 4:2:0 semi-planar
    - YCbCr 4:2:2 planar
    - YCbCr 4:2:2 semi-planar
    - YCbYCr 4:2:2 interleaved
    - YCbCr 4:4:4 planar
    - YCbCr 4:4:4 semi-planar
    - RBG565
    - RBG888
    - ARBG8888
  - Output Bit stream of H.264 "slice_layer_without_partitioning_rbsp()"
  - Output ME results(SAD and MV) for each 16x16 block (optional)
  - Image size is from 128x128 to 4096x2304
  - Maximum frame rate is up to 2560x1440@30fps + 1280x720@30fps

1.1.9 JPEG CODEC

- JPEG codec
  - Input JPEG file : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 sampling formats
  - Output raw image : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
  - Support decode and encode from 48x48 to 8176x8176(66.8Mpixels), step size 8 pixels
  - Support JPEG ROI(region of image) decode
  - Maximum data rate® is up to 76million pixels per second

1.1.10 Image Enhancement (IEP module)

- Image format support
  - Input data: YUV420/YUV422
  - Output data: YUV420/YUV422
  - YUV swap
  - UV SP/P
  - BT601_l/BT601_f/BT709_l/BT709_f color space conversion
  - YUV up/down sampling
- De-interlace
  - 3x5 Y motion detection matrix
  - Source width up to 720x576, 720x480
  - Configured high frequency de-interlace
  - I4O2 (Input 4 field, output 2 frame) /I4O1B/I4O1T/I2O1B/I2O1T mode
- Interface
  - 32bit AHB bus slave
  - 64bit AXI bus master
  - Combined interrupt output

1.1.11 Graphics Engine

- 2D Graphics Engine(RGA module) :
  - Source formats :
    - ABGR8888, XBGR888, ARGB8888, XRGB888
    - RGB888, RGB565
    - RGBA5551, RGBA4444
    - YUV420 planar, YUV420 semi-planar
    - YUV422 planar, YUV422 semi-planar
    - YUV 10-bit for YUV420/422 semi-planar
    - BPP8, BPP4, BPP2, BPP1
  - Destination formats :
    - ABGR8888, XBGR888, ARGB8888, XRGB888
    - RGB888, RGB565
    - RGBA5551, RGBA4444
    - YUV420 planar, YUV420 semi-planar
    - YUV422 planar, YUV422 semi-planar
  - Pixel Format conversion, BT.601/BT.709
  - Max resolution: 8192x8192 source, 4096x4096 destination
  - BitBLT
    - Two source BitBLT:
    - A+B=B only BitBLT, A support rotate & scale when B fixed
    - A+B=C second source (B) has same attribute with (C) plus rotation function
  - Color fill with gradient fill, and pattern fill
  - High-performance stretch and shrink
  - Monochrome expansion for text rendering
  - New comprehensive per-pixel alpha(color/alpha channel separately)
  - Alpha blending modes including Java 2 Porter-Duff compositing blending rules , chroma key, pattern mask, fading
  - Dither operation
  - 0, 90, 180, 270 degree rotation
  - x-mirror, y-mirror & rotation operation

1.1.12 Video OUT

- Display Interface
  - Support HDMI 1.4 output up to 1080p@60Hz
  - TV Interface: TV encoder 10bit out for DAC

- HDMI Interface : 24 bit(RGB888 YCbCr444),
- Max output resolution 1080p for HDMI,720p for MIPI, 480i/576i for CVBS

- Display process
  - Background layer: programmable 24-bit color
  - Win0 layer
    - RGB888, ARGB888, RGB565, YCbCr422, YCbCr420, YCbCr444
    - RB/alpha/mid/uv swap
    - 1/8 to 8 scaling-down and scaling-up engine
    - Support virtual display
    - 256 level alpha blending (pre-multiplied alpha support)
    - Transparency color key
    - De-flicker support for interlace output
    - YCbCr2RGB(rec601-mpeg/ rec601-jpeg/rec709)
    - RGB2YCbCr(BT601/BT709)
  - Win1 layer
    - RGB888, ARGB888, RGB565
    - RB/alpha/endian swap
    - Support virtual display
    - 256 level alpha blending (pre-multiplied alpha support)
    - Transparency color key
    - Direct path support
    - RGB2YCbCr(BT601/BT709)
- Others
  - Win0 layer and Win1 layer overlay exchangeable
  - BCSH(Brightness, Contrast, Saturation, Hue adjustment)
  - BCSH:YCbCr2RGB(rec601-mpeg/ rec601-jpeg/rec709)
  - BCSH:RGB2YCbCr(BT601/BT709)
  - Support Gamma adjust for PAD
  - Support dither down allegro RGB888to666 RGB888to565 & dither down frc (configurable) RGB888to666
  - Blank and black display
  - Standby mode
  - Support RB/RG/BG/delta/dummy swap
  -

1.1.13 HDMI

- Support RGB888 1080p @ 60fps
- HPD input analog comparator
- Compliance HDMI compliance Test specification 1.4
- Support multi-channels PCM or compressed audio transmission (32-192kHz Fs) from I2S, using IEC60958 and IEC 61937

1.1.14 MIPI DSI

- Support RGB888 720p @ 60fps
- Support 4 lanes
- Support command mode
- Compliance MIPI Alliance Standard for Display Pixel Interface (DPI-2)

1.1.15 Audio Interface

- I2S0 with 8ch
  - I2S0 supports up to 8 channels (8xTX, 8xRX)
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)
  - Support 4 PCM formats(early, late1, late2, late3)

- I2S and PCM mode cannot be used at the same time

- I2S1/I2S2(PCM) with 2ch
  - Up to 2 channels (2xTX, 2xRX)
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal , left-justified , right-justified)
  - Support 4 PCM formats(early , late1 , late2 , late3)
  - I2S and PCM cannot be used at the same time
  - I2S1 is connected to HDMI and internal Audio Codec
  - I2S2 is exposed for peripherals

- Audio CODEC
  - 24bit DAC
  - Support Line-out
  - Support Mono, Stereo, 5.1 HiFi channel performance
  - Integrated digital interpolation and decimation filter.
  - Sampling rate of 8kHz/12kHz/16kHz/24kHz/32kHz/44.1KHz/48KHz/96KHz
  - Optional fractional PLL available that support 6MHz to 20MHz clock input to any clock
  - Support PCM/I2S Mode
  - Support MIC single-ended/double-ended difference input

1.1.16 Connectivity

- SDIO interface
  - Compatible with SDIO 3.0 protocol
  - 4bits data bus widths

- MAC 10/100M Ethernet Controller
  - Supports 10/100-Mbps data transfer rates with the RMII interfaces
  - Supports both full-duplex and half-duplex operation
    - Supports CSMA/CD Protocol for half-duplex operation
    - Supports IEEE 802.3x flow control for full-duplex operation
    - Optional forwarding of received pause control frames to the user application in full-duplex operation
    - Back-pressure support for half-duplex operation
    - Automatic transmission of zero-quanta pause frame on de-assertion of flow control input in full-duplex operation
  - Preamble and start-of-frame data (SFD) insertion in Transmit, and deletion in Receive paths
  - Automatic CRC and pad generation controllable on a per-frame basis
  - Options for Automatic Pad/CRC Stripping on receive frames
  - Programmable Inter-Frame-Gap (40-96 bit times in steps of 8)
  - Supports a variety of flexible address filtering modes
  - Separate 32-bit status returned for transmission and reception packets
  - Supports IEEE 802.1Q VLAN tag detection for reception frames
  - Support detection of LAN wake-up frames and AMD Magic Packet frames
  - Support checksum off-load for received IPv4 and TCP packets encapsulated by the Ethernet frame
  - Support checking IPv4 header checksum and TCP, UDP, or ICMP checksum encapsulated in IPv4 or IPv6 datagram
  - Comprehensive status reporting for normal operation and transfers with errors
  - Automatic generation of PAUSE frame control or backpressure signal to the GMAC core based on Receive FIFO-fill (threshold configurable) level
  - Handles automatic retransmission of Collision frames for transmission
  - Discards frames on late collision, excessive collisions, excessive deferral and under-

run conditions

- SPI Controller
  - Support serial-master and serial-slave mode, software-configurable
  - DMA-based or interrupt-based operation
  - Embedded two 32x16bits FIFO for TX and RX operation respectively
  - Support 2 chip-selects output in serial-master mode

- SFC
  - Support one chip select
  - Support x1,x2,x4 data bits mode
  - Support interrupt output, interrupt maskable
  - Support Spansion, MXIC, Gigadevice …vendor's nor flash memory.

- UART Controller
  - 3 on-chip UART controller inside RV1108
  - DMA-based or interrupt-based operation
  - UART1/1/2 Embedded two 64Bytes FIFO for TX and RX operation respectively
  - Support 5bit,6bit,7bit,8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start, stop and parity
  - Support different input clock for UART operation to get up to 4Mbps or other special baud rate
  - Support non-integer clock divides for baud clock generation
  - Support auto flow control mode

- I2C controller
  - 4 on-chip I2C controller in RV1108
  - Multi-master I2C operation
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency and transfer rate up to 400Kbit/s in the fast mode
  - Serial 8bits oriented and bidirectional data transfers can be made at up to 100Kbit/s in the standard mode

- GPIO
  - 4 groups of GPIO (GPIO0~GPIO3) , 32 GPIOs per group in GPIO0~GPIO3, totally have 128 GPIOs
  - All of GPIOs can be used to generate interrupt to Cortex-A7
  - All of pull-up GPIOs are software-programmable for pull-up resistor or not
  - All of pull-down GPIOs are software-programmable for pull-down resistor
  - or not
  - All of GPIOs are always in input direction in default after power-on-reset

- USB Host2.0
  - Embedded 3 USB Host 2.0 interfaces
  - Compatible with USB Host2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Provides 16 host mode channels
  - Support periodic out channel in host mode

- USB OTG2.0
  - Compatible with USB OTG2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Support up to 9 device mode endpoints in addition to control endpoint 0
  - Support up to 6 device mode IN endpoints including control endpoint 0
  - Endpoints 1/3/5/7 can be used only as data IN endpoint

- Endpoints 2/4/6 can be used only as data OUT endpoint
- Endpoints 8/9 can be used as data OUT and IN endpoint
- Provides 9 host mode channels

1.1.17 Others

- Temperature Sensor(TS-ADC)
  - 10-bits ADC up to 50KS/s sampling rate
  - -40~125℃ temperature range and 5℃ temperature resolution

- Successive Approximation ADC (SARADC)
  - 10-bit resolution
  - Up to 1MS/s sampling rate
  - 6 single-ended input channels
  - Current consumption: 0.5mA @ 1MS/s

- eFuse
  - Two high-density electrical Fuse is integrated: two 256bits (32x8)
  - Support standby mode
  - Provide inactive mode, VP must be 0V or Floating in this mode.

- Package Type
  - BGA359 (body: 14mm x 14mm; ball size: 0.3mm; ball pitch: 0.65mm)
  - RV1108G embedded 128M DDR3-1600.

Notes :
① *DDR3 are not used simultaneously*
② *Actual maximum frame rate will depend on the clock frequency and system bus performance*
③ *Actual maximum data rate will depend on the clock frequency and JPEG compression rate*

1.2 Block Diagram

The following diagram shows the basic block diagram for RV1108

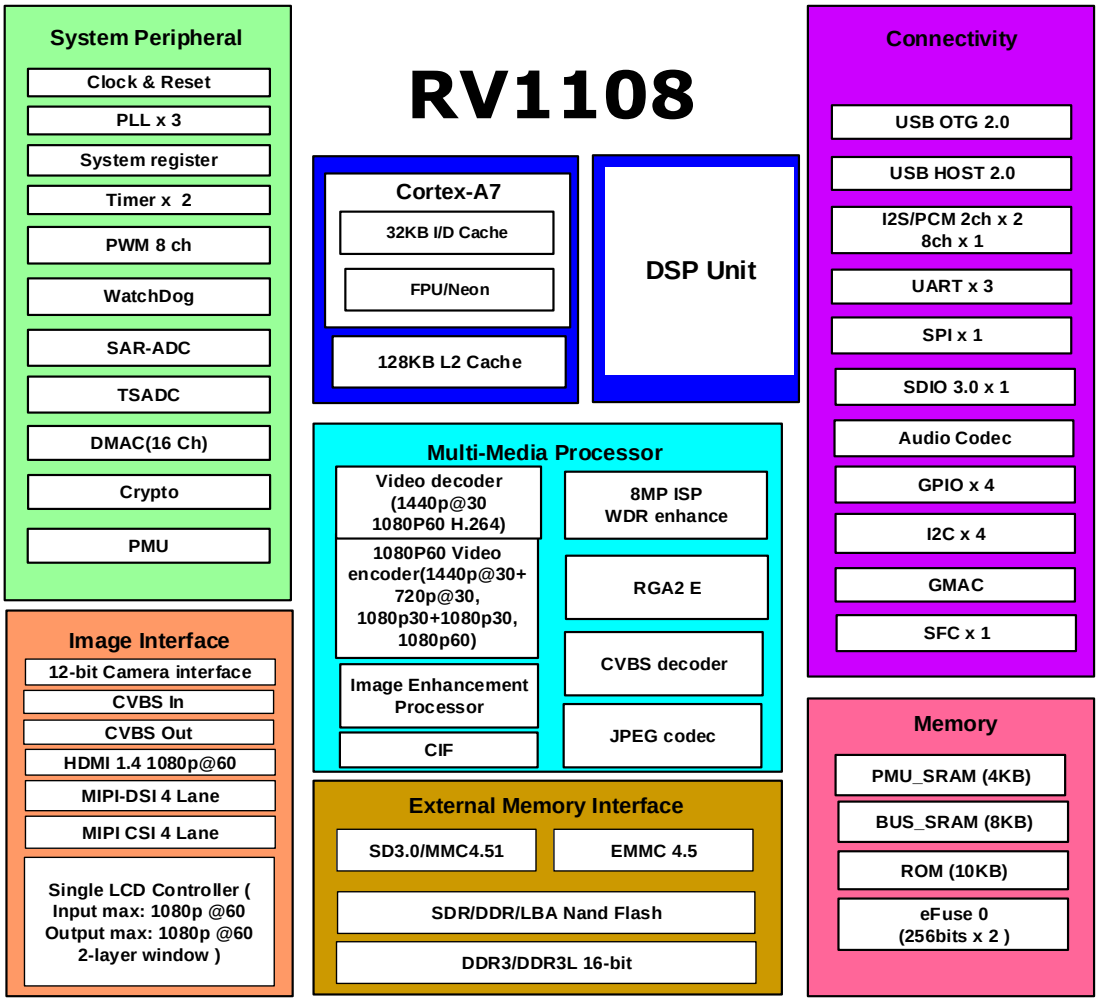


Fig. 1-1 RV1108 Block Diagram

Chapter 2 Package Information

2.1 Ordering information

Orderable Device	ROHS Status	Package	Package Qty	Device Feature
RV1108A	ROHS	BGA359	1190pcs by tray	Cortex A7 + DSP SoC
RV1108G	ROHS	BGA359	1190pcs by tray	Cortex A7 + DSP with 128MB DDR3
RV1108K1	ROHS	BGA359	1190pcs by tray	Cortex A7 + DSP SoC for industrial application

2.2 Top Marking

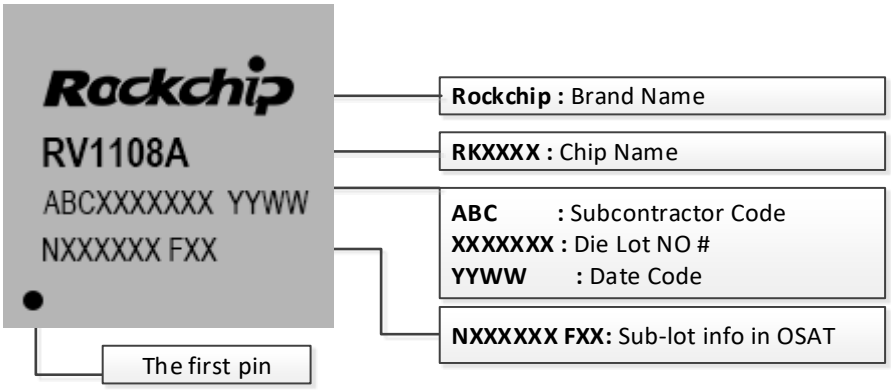


Fig. 2-1 RV1108A Silk Marking

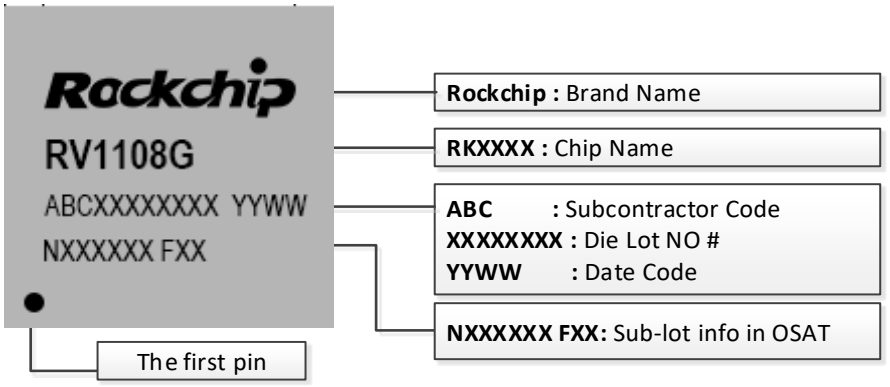


Fig. 2-2 RV1108G Silk Marking

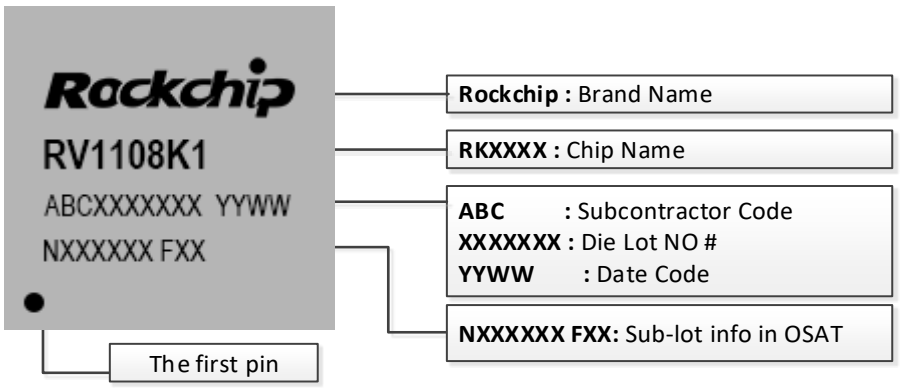
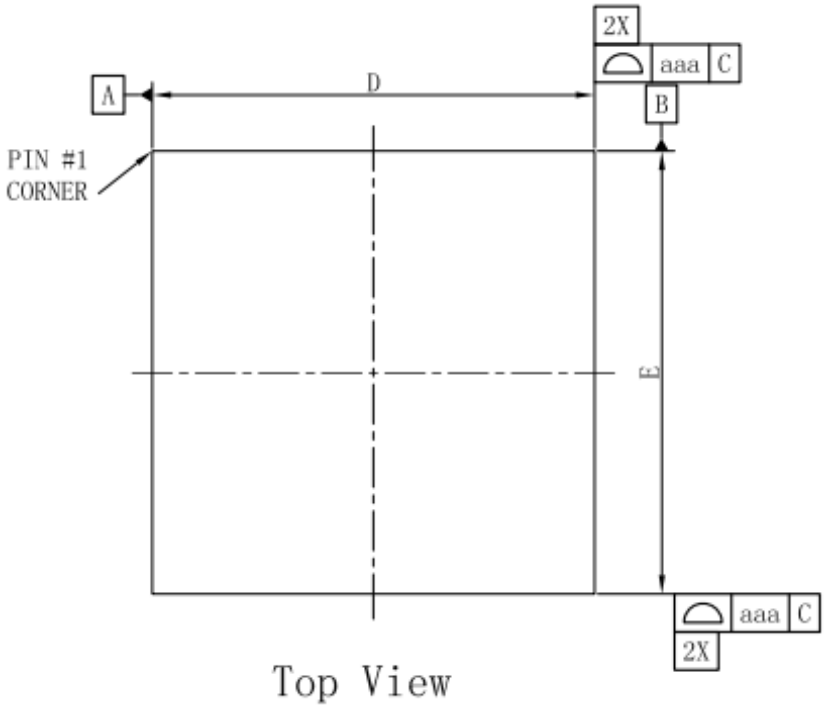


Fig. 2-3 RV1108K Silk Marking

2.3 Dimension



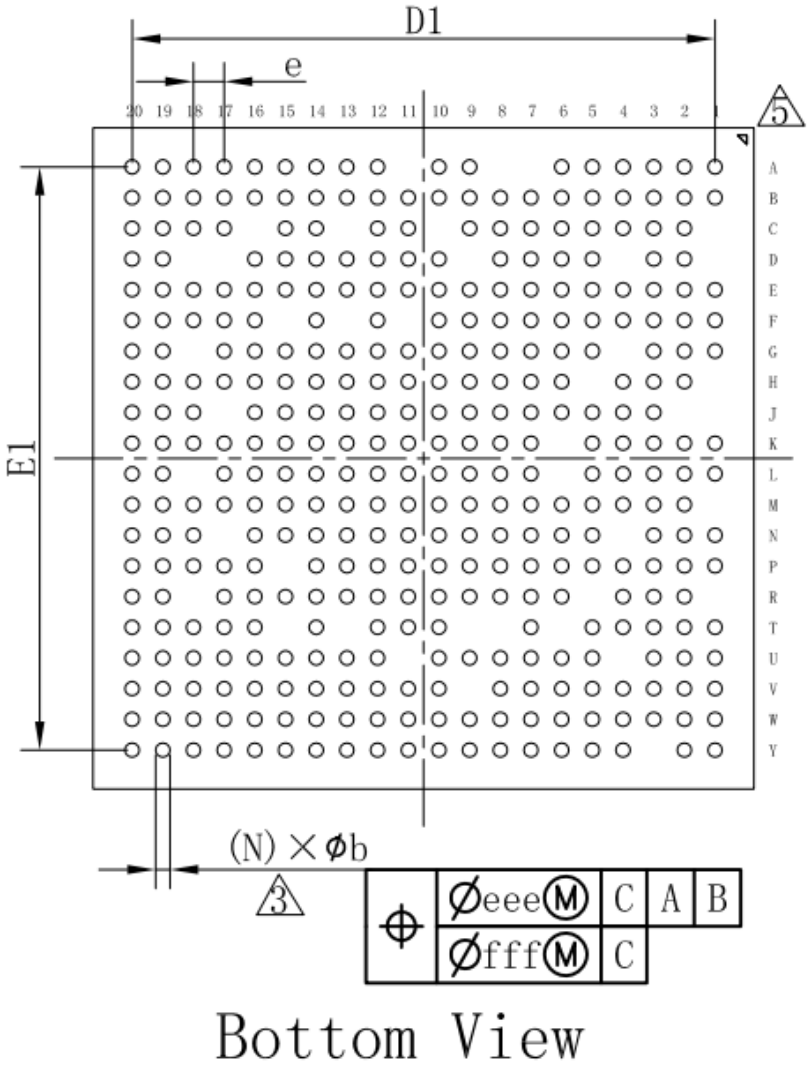
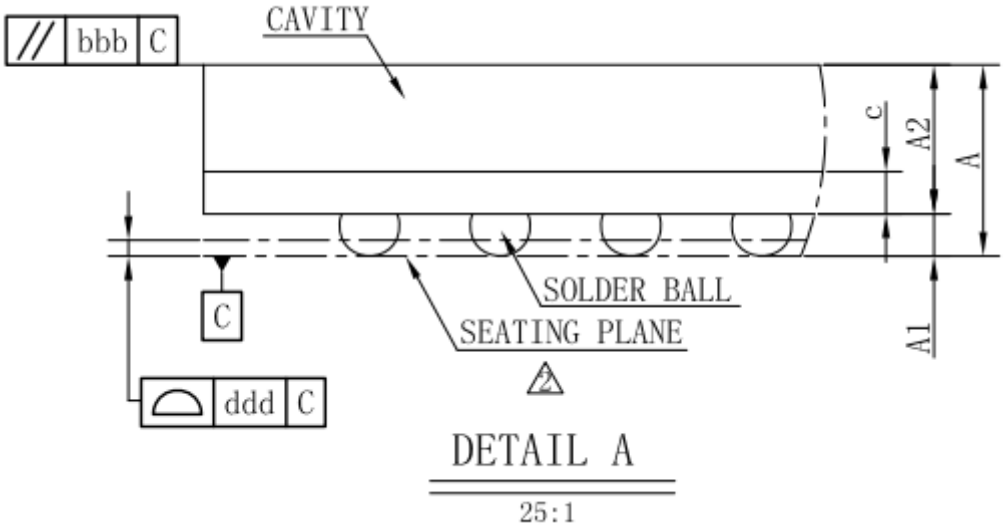
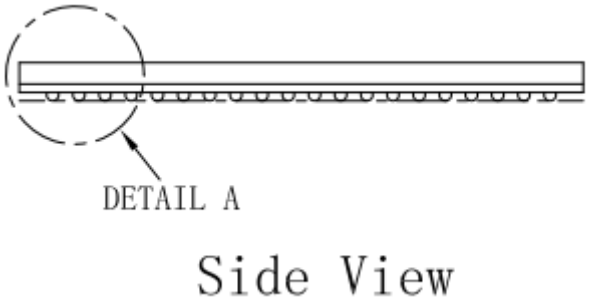


Fig. 2-4 RV1108 BGA359 Package Top View and bottom view





Side View

Fig. 2-5 RV1108 BGA359 Package Side View

symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.100	---	---	0.043
A1	0.160	0.210	0.260	0.006	0.008	0.010
A2	0.690	0.740	0.810	0.027	0.029	0.032
c	0.170	0.210	0.250	0.007	0.008	0.010
D	13.900	14.000	14.100	0.547	0.551	0.555
E	13.900	14.000	14.100	0.547	0.551	0.555
D1	---	12.350	---	---	0.486	---
E1	---	12.350	---	---	0.486	---
e	---	0.650	---	---	0.026	---
b	0.250	0.300	0.350	0.010	0.012	0.014
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.080			0.003		
Ball Diam	0.300			0.012		
N	359			359		
MD/ME	20/20			20/20		

Fig. 2-6 RV1108 BGA359 Package Dimension

2.4 Ball Map

400	1	2	3	4	5	6	7	8	9	10	11	12
A	VSS_1	DDR_A7	DDR_A2	VSS_89	DDR_A14	DDR_A6			VSS_95	DDR_A8		GPIO3_C2/SDMMC0_D1/UART2_RX
B	DDR_CS0N	DDR_BA0	DDR_A5	DDR_A0	DDR_A11	DDR_A4	DDR_A12	VSS_98	DDR_CKE	DDR_A1	SADC_AVDD_1V8	GPIO3_C3/SDMMC0_D0/UART2_TX
C		DDR_CLKN	DDR_CLK	VSS_97	DDR_ODT0	VSS_90	VSS_96	DDR_BA1	DDR_A10		VSS_72	GPIO3_C0/SDMMC0_D3
D		VSS_88	DDR_DQ4		DDR_RASN	DDR_BA2	DDR_A13	DDR_CASN		ADC_IN3	GPIO3_B7/SDMMC0_PWR	GPIO3_C1/SDMMC0_D2
E	VSS_85	DDR_DQ1	DDR_DQ7	FP_1	VSS_100	DDR_A3	DDR_A9	DDR_WEN	VSS_93	DDR_VDD_4	ADC_IN5	ADC_IN2
F	DDR_DQ3	VSS_87	DDR_DQ0	DDR_DQ6	DDR_RESET	FP_2	DDR_VDD_5	DDR_VDD_6	DDR_VDD_7	VSS_11		ADC_IN4
G	DDR_DM0	DDR_DQ5	VSS_86		DDR_DQ2	DDR_VDD_3	VSS_37	CORE_VDD_1	CORE_VDD_2	VSS_8	VSS_92	VSS_102
H		DDR_DQS1	DDR_DQS1N	DDR_DQ13		DDR_VDD_2	VSS_91	VSS_14	VSS_15	VSS_16	VSS_17	VSS_18
J			DDR_DQS0	DDR_DQ9	VSS_73	DDR_VDD_1	CORE_VDD_7	VSS_22	VSS_23	VSS_24	VSS_25	VSS_26
K	VSS_99	DDR_DQ8	VSS_4	DDR_DQS0N	DDR_DQ12		VSS_29	VSS_30	VSS_31	VSS_32	VSS_33	VSS_34
L	DDR_DQ15	DDR_DQ11	DDR_DM1	DDR_DQ14	VSS_13		VSS_5	VSS_38	VSS_39	VSS_40	VSS_41	VSS_42
M		DDR_DQ10	GPIO0_A7/SPI_TXD	GPIO0_C0/PWM3/IR	GPIO0_B7/TSADC_SHUT	PLL_AVDD_1V0	VSS_45	VSS_46	VSS_47	VSS_48	VSS_49	VSS_50

13	14	15	16	17	18	19	20	
GPIO3_C5/SDMMC0_CMD	VIDEO_INP	CODEC_AOL	CODEC_AOR	CODEC_MICBIAS	GPIO1_D0/UART1_CTSN/SPI_CLK/DSP_TCK	GPIO1_D1/UART1_RTSN/SPI_CSN0/DSP_TMS	GPIO1_D7/HDMI_CEC/DSP_RTCK	A
GPIO3_C4/SDMMC0_CLKO	VIDEO_INN	CODEC_MICR	CODEC_VCM	VSS_6	GPIO1_D3/UART1_TX/SPI_TXD/DSP_TDO	VSS_2	GPIO1_B3/LCDC_D16/I2S_SCLK/GMAC_TXD1	B
	VIDEO_AVDD_1V8	CODEC_MICL		5VGPIO1_D5/UART2_RTSN/HDMI_I2C0_SDA	5VGPIO1_D6/HDMI_HPD0	GPIO1_B4/LCDC_D15/I2S_MCLK/GMAC_TXEN	GPIO1_B6/LCDC_D13/I2S_LRCLKTX/GMAC_RXD1	C
ADC_IN0	VSS_69	CODEC_AVDD_1V8	VSS_60			GPIO1_D2/UART1_RX/SPI_RXD	GPIO1_C2/LCDC_DEN/I2S_SDIO3/GMAC_RXER	D
ADC_IN1	VIDEO_AVDD_1V0	CODEC_AVSS	GPIO2_D2/UART2_TX/JTAG_TCK	5VGPIO1_D4/UART2_CTSN/HDMI_I2C0_SCL	GPIO1_C0/LCDC_D11/I2S_LRCLKRX	GPIO1_C1/LCDC_D10/I2S_SDI/PWM4	GPIO1_C3/LCDC_VSYNC/GMAC_MDIO	E
	APIO3_VDD		GPIO2_D1/UART2_RX/JTAG_TMS	GPIO1_B2/LCDC_D17/I2S_SDO/GMAC_TXD0	GPIO1_B5/LCDC_D14/I2S_SDIO1/GMAC_RXD0	GPIO1_C4/LCDC_HSYNC/GMAC_MDC	GPIO2_B1/FLASH_CLE	F
VSS_7	VSS_10	CORE_VDD_4	GPIO1_B7/LCDC_D12/I2S_SDIO2/GMAC_RXDV	GPIO1_C5/LCDC_CLK/GMAC_CLK		GPIO2_B4/FLASH_RDY/EMMC_CMD/SFC_CSN0	GPIO2_A4/FLASH_D4/EMMC_D4	G
VSS_19	VSS_20	VSS_105	APIO1_VDD	GPIO2_C2/FLASH_WP/EMMC_PWR	GPIO2_B0/FLASH_ALE	GPIO2_A3/FLASH_D3/EMMC_D3/SFC_HOLD_IO3	GPIO2_A7/FLASH_D7/EMMC_D7	H
VSS_27	VSS_103	CORE_VDD_3	GPIO2_A1/FLASH_D1/EMMC_D1/SFC_SIO_IO1		GPIO2_B7/FLASH_CSN1/SFC_CLK	GPIO2_A5/FLASH_D5/EMMC_D5	GPIO2_B5/FLASH_CSN0	J
VSS_35	VSS_36	VSS_106	APIO6_VDD	GPIO2_A2/FLASH_D2/EMMC_D2/SFC_WP_IO2	GPIO2_A0/FLASH_D0/EMMC_D0/SFC_SIO_IO0	GPIO2_B2/FLASH_WRN	GPIO2_B6/EMMC_CLKO	K
VSS_43	VSS_28	CORE_VDD_6	GPIO2_A6/FLASH_D6/EMMC_D6	GPIO2_B3/FLASH_RDN		GPIO2_D7/SDIO_D0	GPIO2_D6/SDIO_CMD	L
VSS_51	VSS_52	VSS_70	VSS_104	GPIO3_A2/SDIO_D3	GPIO3_A0/SDIO_D1	GPIO2_D5/SDIO_CLKO	GPIO3_A1/SDIO_D2	M

	1	2	3	4	5	6	7	8	9	10	11	12
N	GPIO0_B6/I2C3_SCL	VSS_74	EFUSE		GPIO0_B5/PMIC_SLEEP	PLL_AVDD_1V8	VSS_53	VSS_54	VSS_55	VSS_56	VSS_57	VSS_58
P	XIN_24M	XOUT24M	VSS_61	GPIO0_A3/SPI_CLK	GPIO0_A4/SPI_CSN0	GPIO0_C3/PMU_DEBUG2	TEST	VSS_62	VSS_63	VSS_64	VSS_65	VSS_66
R		GPIO0_B3	GPIO0_C6/PWM2/I2C2_SCL/PMU_DEBUG4	GPIO0_B2/I2C0_SDA		PMU_DVDD_1V0	CORE_VDD_8	PMUIO_VDD	VSS_71	VSS_44	VSS_101	VSS_9
T	NPOR	GPIO0_C5/PWM0/PMU_DEBUG3	GPIO0_C4/PWM1/I2C3_SDA	GPIO0_B1/I2C0_SCL	GPIO0_B4		GPIO0_A1/SDMMC0_DET			USB_AVDD_1V8	USB_AVDD_3V3	USB_VDD_1V0
U	GPIO0_A2/SDMMC1_PWR	GPIO0_C2/I2C2_SDA/PMU_DEBUG1	GPIO0_C1/HDMI_HPD1/CVBS_CLK_IN		GPIO0_B0/SPI_RXD	HDMI_EXTR	VDAC_AVDD_1V8	MIPI_DSI_AVDD_1V8	MIPI_DSI_AVDD_3V3	USB_EXTR		MIPI_CSI_EXTR
V	GPIO0_A6/PMU_DEBUG0	GPIO0_A5/CLK_WIFI_OUT	HDMI_AVDD_1V8	VSS_78	HDMI_AVDD_1V0	VSS_79	MIPI_DSI_AVDD_1V0	VSS_80		VSS_81	USB0_ID	USB_VBUS
W	HDMI_TXCP	HDMI_TX0N	HDMI_TX0P	HDMI_TX1N	HDMI_TX2P	VDAC_EXTR	GPIO1_B1/LCDC_D9/MIPI_D3N/PWM7	GPIO1_A7/LCDC_D7/MIPI_D2N/PWM5	GPIO1_A1/LCDC_D5/MIPI_CLKN	GPIO1_A4/LCDC_D3/MIPI_D1P	GPIO1_A2/LCDC_D1/MIPI_D0P	USB0_DP
Y	HDMI_TXCN	VSS_77		HDMI_TX1P	HDMI_TX2N	VDAC_OUT	GPIO1_B0/LCDC_D8/MIPI_D3P/PWM6	GPIO1_A6/LCDC_D6/MIPI_D2P	GPIO1_A0/LCDC_D4/MIPI_CLKP	GPIO1_A5/LCDC_D2/MIPI_D1N	GPIO1_A3/LCDC_D0/MIPI_D0N	USB0_DM

VSS_59	VSS_12	CORE_VDD_5	GPIO3_B1/PCM_OUT/FLASH_TRIG_OUT		GPIO3_B2/PCM_IN/FLASH_TRIG_IN	GPIO3_B6	GPIO3_B4/PCM_SYNC/PRELIGHT_TRIG_OUT	**N**
VSS_67	VSS_68		APIO5_VDD	GPIO3_A6/UART0_TX	GPIO3_A4/UART0_CTSN	GPIO3_A7	GPIO3_B5/MIPI_CSI_MCLK	**P**
VSS_75	VSS_76	VSS_94	GPIO3_D5/CIF_D10/FLASH_TRIG_OUT	GPIO2_D4/I2C1_SCL		GPIO3_B3/PCM_CLK	GPIO3_A3/UART0_RTSN	**R**
	VSS_21		APIO2_VDD	GPIO3_D1/CIF_PDN	GPIO3_C7/CIF_CLKIN	GPIO2_D3/I2C1_SDA	GPIO3_A5/UART0_RX	**T**
MIPI_CSI_AVDD_1V0	GPIO2_C1/CIF_D7/I2S_SDI	GPIO2_C5/CIF_D2/I2S_MCLK	GPIO2_C4/CIF_D1/I2S_SCLK	GPIO3_D4/CIF_D9/FLASH_TRIG_IN	GPIO3_D0/CIF_HREF	GPIO1_C7/CIF_D5/I2S_SDIO2	GPIO3_B0	**U**
VSS_82	GPIO2_C6/CIF_D3/I2S_SDIO1	VSS_83	GPIO2_C3/CIF_D0/I2S_SDO	VSS_84	GPIO3_D2/CIF_CLKOUT	GPIO3_C6/CIF_VSYNC	GPIO1_C6/CIF_D4//I2S_LRCLKTX	**V**
USB1_DP	MIPI_CSI_D0N	MIPI_CSI_D1N	MIPI_CSI_CLKP	MIPI_CSI_D2N	MIPI_CSI_D3P	VSS_3	GPIO3_D6/CIF_D11/PRELIGHT_TRIG_OUT	**W**
USB1_DM	MIPI_CSI_D0P	MIPI_CSI_D1P	MIPI_CSI_CLKN	MIPI_CSI_D2P	MIPI_CSI_D3N	GPIO2_C0/CIF_D6/I2S_LRCLKRX	GPIO3_D3/CIF_D8/I2S_SDIO3	**Y**
13	**14**	**15**	**16**	**17**	**18**	**19**	**20**	

Fig. 2-7 RV1108A BGA 359 Ball Map

400	1	2	3	4	5	6	7	8	9	10	11
A	VSS_1	VSS_107	VSS_108	VSS_89	DDR_VDD_15	VSS_115			VSS_95	DDR_VDD_23	
B	VSS_109	VSS_110	VSS_111	VSS_112	DDR_VDD_16	VSS_113	VSS_114	VSS_98	VSS_116	DDR_VDD_24	SADC_AVDD_1V8
C		DDR_VDD_12	DDR_VDD_13	VSS_97	DDR_VDD_17	VSS_90	VSS_96	DDR_VDD_22	VSS_117		VSS_72
D		VSS_88	DDR_VDD_14		DDR_VDD_18	DDR_VDD_19	DDR_VDD_20	DDR_VDD_21		ADC_IN3	GPIO3_B7/SDMMC0_PWR
E	VSS_85	VSS_122	VSS_123	PZQ	VSS_100	DDR_VDD_25	DDR_VDD_26	DDR_VDD_27	VSS_93	DDR_VDD_4	ADC_IN5
F	VSS_121	VSS_87	VSS_124	VSS_125	VSS_126	VREF	DDR_VDD_5	DDR_VDD_6	DDR_VDD_7	VSS_11	
G	VSS_118	VSS_119	VSS_86		DDR_VDD_11	DDR_VDD_3	VSS_37	CORE_VDD_1	CORE_VDD_2	VSS_8	VSS_92
H		DDR_VDD_8	DDR_VDD_9	DDR_VDD_10		DDR_VDD_2	VSS_91	VSS_14	VSS_15	VSS_16	VSS_17
J			VSS_127	VSS_128	VSS_73	DDR_VDD_1	CORE_VDD_7	VSS_22	VSS_23	VSS_24	VSS_25

12	13	14	15	16	17	18	19	20	
GPIO3_C2/SDMMC0_D1/UART2_RX	GPIO3_C5/SDMMC0_CMD	VIDEO_INP	CODEC_AOL	CODEC_AOR	CODEC_MICBIAS	GPIO1_D0/UART1_CTSN/SPI_CLK/DSP_TCK	GPIO1_D1/UART1_RTSN/SPI_CSN0/DSP_TMS	GPIO1_D7/HDMI_CEC/DSP_RTCK	**A**
GPIO3_C3/SDMMC0_D0/UART2_TX	GPIO3_C4/SDMMC0_CLKO	VIDEO_INN	CODEC_MICR	CODEC_VCM	VSS_6	GPIO1_D3/UART1_TX/SPI_TXD/DSP_TDO	VSS_2	GPIO1_B3/LCDC_D16/I2S_SCLK/GMAC_TXD1	**B**
GPIO3_C0/SDMMC0_D3		VIDEO_AVDD_1V8	CODEC_MICL		5VGPIO1_D5/UART2_RTSN/HDMI_I2C0_SDA	5VGPIO1_D6/HDMI_HPD0	GPIO1_B4/LCDC_D15/I2S_MCLK/GMAC_TXEN	GPIO1_B6/LCDC_D13/I2S_LRCLKTX/GMAC_RXD1	**C**
GPIO3_C1/SDMMC0_D2	ADC_IN0	VSS_69	CODEC_AVDD_1V8	VSS_60			GPIO1_D2/UART1_RX/SPI_RXD	GPIO1_C2/LCDC_DEN/I2S_SDIO3/GMAC_RXER	**D**
ADC_IN2	ADC_IN1	VIDEO_AVDD_1V0	CODEC_AVSS	GPIO2_D2/UART2_TX/JTAG_TCK	5VGPIO1_D4/UART2_CTSN/HDMI_I2C0_SCL	GPIO1_C0/LCDC_D11/I2S_LRCLKRX	GPIO1_C1/LCDC_D10/I2S_SDI/PWM4	GPIO1_C3/LCDC_VSYNC/GMAC_MDIO	**E**
ADC_IN4		APIO3_VDD		GPIO2_D1/UART2_RX/JTAG_TMS	GPIO1_B2/LCDC_D17/I2S_SDO/GMAC_TXD0	GPIO1_B5/LCDC_D14/I2S_SDIO1/GMAC_RXD0	GPIO1_C4/LCDC_HSYNC/GMAC_MDC	GPIO2_B1/FLASH_CLE	**F**
VSS_102	VSS_7	VSS_10	CORE_VDD_4	GPIO1_B7/LCDC_D12/I2S_SDIO2/GMAC_RXDV	GPIO1_C5/LCDC_CLK/GMAC_CLK		GPIO2_B4/FLASH_RDY/EMMC_CMD/SFC_CSN0	GPIO2_A4/FLASH_D4/EMMC_D4	**G**
VSS_18	VSS_19	VSS_20	VSS_105	APIO1_VDD	GPIO2_C2/FLASH_WP/EMMC_PWR	GPIO2_B0/FLASH_ALE	GPIO2_A3/FLASH_D3/EMMC_D3/SFC_HOLD_IO3	GPIO2_A7/FLASH_D7/EMMC_D7	**H**
VSS_26	VSS_27	VSS_103	CORE_VDD_3	GPIO2_A1/FLASH_D1/EMMC_D1/SFC_SIO_IO1		GPIO2_B7/FLASH_CSN1/SFC_CLK	GPIO2_A5/FLASH_D5/EMMC_D5	GPIO2_B5/FLASH_CSN0	**J**

K	VSS_99	VSS_129	VSS_4	VSS_130	VSS_135		VSS_29	VSS_30	VSS_31	VSS_32	VSS_33
L	VSS_131	VSS_132	VSS_133	VSS_120	VSS_13		VSS_5	VSS_38	VSS_39	VSS_40	VSS_41
M		VSS_134	GPIO0_A7/SPI_TXD	GPIO0_C0/PWM3/IR	GPIO0_B7/TSADC_SHUT	PLL_AVDD_1V0	VSS_45	VSS_46	VSS_47	VSS_48	VSS_49
N	GPIO0_B6/I2C3_SCL	VSS_74	EFUSE		GPIO0_B5/PMIC_SLEEP	PLL_AVDD_1V8	VSS_53	VSS_54	VSS_55	VSS_56	VSS_57
P	XIN_24M	XOUT24M	VSS_61	GPIO0_A3/SPI_CLK	GPIO0_A4/SPI_CSN0	GPIO0_C3/PMU_DEBUG2	TEST	VSS_62	VSS_63	VSS_64	VSS_65
R		GPIO0_B3	GPIO0_C6/PWM2/I2C2_SCL/PMU_DEBUG4	GPIO0_B2/I2C0_SDA		PMU_DVDD_1V0	CORE_VDD_8	PMUIO_VDD	VSS_71	VSS_44	VSS_101
T	NPOR	GPIO0_C5/PWM0/PMU_DEBUG3	GPIO0_C4/PWM1/I2C3_SDA	GPIO0_B1/I2C0_SCL	GPIO0_B4		GPIO0_A1/SDMMC0_DET			USB_AVDD_1V8	USB_AVDD_3V3
U	GPIO0_A2/SDMMC1_PWR	GPIO0_C2/I2C2_SDA/PMU_DEBUG1	GPIO0_C1/HDMI_HPD1/CVBS_CLK_IN		GPIO0_B0/SPI_RXD	HDMI_EXTR	VDAC_AVDD_1V8	MIPI_DSI_AVDD_1V8	MIPI_DSI_AVDD_3V3	USB_EXTR	
V	GPIO0_A6/PMU_DEBUG0	GPIO0_A5/CLK_WIFI_OUT	HDMI_AVDD_1V8	VSS_78	HDMI_AVDD_1V0	VSS_79	MIPI_DSI_AVDD_1V0	VSS_80		VSS_81	USB0_ID
W	HDMI_TXCP	HDMI_TX0N	HDMI_TX0P	HDMI_TX1N	HDMI_TX2P	VDAC_EXTR	GPIO1_B1/LCDC_D9/MIPI_D3N/PWM7	GPIO1_A7/LCDC_D7/MIPI_D2N/PWM5	GPIO1_A1/LCDC_D5/MIPI_CLKN	GPIO1_A4/LCDC_D3/MIPI_D1P	GPIO1_A2/LCDC_D1/MIPI_D0P
Y	HDMI_TXCN	VSS_77		HDMI_TX1P	HDMI_TX2N	VDAC_OUT	GPIO1_B0/LCDC_D8/MIPI_D3P/PWM6	GPIO1_A6/LCDC_D6/MIPI_D2P	GPIO1_A0/LCDC_D4/MIPI_CLKP	GPIO1_A5/LCDC_D2/MIPI_D1N	GPIO1_A3/LCDC_D0/MIPI_D0N
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**

VSS_34	VSS_35	VSS_36	VSS_106	APIO6_VDD	GPIO2_A2/FLASH_D2/EMMC_D2/SFC_WP_IO2	GPIO2_A0/FLASH_D0/EMMC_D0/SFC_SIO_IO0	GPIO2_B2/FLASH_WRN	GPIO2_B6/EMMC_CLKO	K
VSS_42	VSS_43	VSS_28	CORE_VDD_6	GPIO2_A6/FLASH_D6/EMMC_D6	GPIO2_B3/FLASH_RDN		GPIO2_D7/SDIO_D0	GPIO2_D6/SDIO_CMD	L
VSS_50	VSS_51	VSS_52	VSS_70	VSS_104	GPIO3_A2/SDIO_D3	GPIO3_A0/SDIO_D1	GPIO2_D5/SDIO_CLKO	GPIO3_A1/SDIO_D2	M
VSS_58	VSS_59	VSS_12	CORE_VDD_5	GPIO3_B1/PCM_OUT/FLASH_TRIG_OUT		GPIO3_B2/PCM_IN/FLASH_TRIG_IN	GPIO3_B6	GPIO3_B4/PCM_SYNC/PRELIGHT_TRIG_OUT	N
VSS_66	VSS_67	VSS_68		APIO5_VDD	GPIO3_A6/UART0_TX	GPIO3_A4/UART0_CTSN	GPIO3_A7	GPIO3_B5/MIPI_CSI_MCLK	P
VSS_9	VSS_75	VSS_76	VSS_94	GPIO3_D5/CIF_D10/FLASH_TRIG_OUT	GPIO2_D4/I2C1_SCL		GPIO3_B3/PCM_CLK	GPIO3_A3/UART0_RTSN	R
USB_VDD_1V0		VSS_21		APIO2_VDD	GPIO3_D1/CIF_PDN	GPIO3_C7/CIF_CLKIN	GPIO2_D3/I2C1_SDA	GPIO3_A5/UART0_RX	T
MIPI_CSI_EXTR	MIPI_CSI_AVDD_1V0	GPIO2_C1/CIF_D7/I2S_SDI	GPIO2_C5/CIF_D2/I2S_MCLK	GPIO2_C4/CIF_D1/I2S_SCLK	GPIO3_D4/CIF_D9/FLASH_TRIG_IN	GPIO3_D0/CIF_HREF	GPIO1_C7/CIF_D5/I2S_SDIO2	GPIO3_B0	U
USB_VBUS	VSS_82	GPIO2_C6/CIF_D3/I2S_SDIO1	VSS_83	GPIO2_C3/CIF_D0/I2S_SDO	VSS_84	GPIO3_D2/CIF_CLKOUT	GPIO3_C6/CIF_VSYNC	GPIO1_C6/CIF_D4//I2S_LRCLKTX	V
USB0_DP	USB1_DP	MIPI_CSI_D0N	MIPI_CSI_D1N	MIPI_CSI_CLKP	MIPI_CSI_D2N	MIPI_CSI_D3P	VSS_3	GPIO3_D6/CIF_D11/PRELIGHT_TRIG_OUT	W
USB0_DM	USB1_DM	MIPI_CSI_D0P	MIPI_CSI_D1P	MIPI_CSI_CLKN	MIPI_CSI_D2P	MIPI_CSI_D3N	GPIO2_C0/CIF_D6/I2S_LRCLKRX	GPIO3_D3/CIF_D8/I2S_SDIO3	Y
12	13	14	15	16	17	18	19	20	

Fig. 2-8 RV1108G BGA 359 Ball Map

Notes:

The pins of RV1108G are different from RV1108A, as follows:
A2,A3 ,A6 ,B1,B2,B3,B4 ,B6,B7,B9,C9,E2,E3,F1,F3,F4,F5,G1,G2,J3,J4,K2,K4,K5,L1,L2,L3,L4,M2 are GND.

A5,A10,B5,B10,C2,C3,C5,C8,D3,D5,D6,D7,D8,E6,E7,E8 ,G5, H2,H3,H4 are DDR_VDD.

E4 is PZQ, F6 is VREF. As fig.2-8.

2.5 Pin List

Table 2-1 RV1108A BGA359 Pin List

Pin #	Pin Name	Pin #	Pin Name
A5	DDR_A14	H19	GPIO2_A3/FLASH_D3/EMMC_D3/SFC_HOLD_IO3
D7	DDR_A13	J16	GPIO2_A1/FLASH_D1/EMMC_D1/SFC_SIO_IO1
F5	DDR_RESET	G20	GPIO2_A4/FLASH_D4/EMMC_D4
A10	DDR_A8	H18	GPIO2_B0/FLASH_ALE
A2	DDR_A7	G19	GPIO2_B4/FLASH_RDY/EMMC_CMD/SFC_CSN0
A6	DDR_A6	F20	GPIO2_B1/FLASH_CLE
E7	DDR_A9	H17	GPIO2_C2/FLASH_WP/EMMC_PWR
B5	DDR_A11	H16	APIO1_VDD
A3	DDR_A2	G17	GPIO1_C5/LCDC_CLK/GMAC_CLK
B6	DDR_A4	F19	GPIO1_C4/LCDC_HSYNC/GMAC_MDC
B3	DDR_A5	E20	GPIO1_C3/LCDC_VSYNC/GMAC_MDIO
B10	DDR_A1	D20	GPIO1_C2/LCDC_DEN/I2S_SDIO3/GMAC_RXER
E6	DDR_A3	E19	GPIO1_C1/LCDC_D10/I2S_SDI/PWM4
B7	DDR_A12	E18	GPIO1_C0/LCDC_D11/I2S_LRCLKRX
B4	DDR_A0	G16	GPIO1_B7/LCDC_D12/I2S_SDIO2/GMAC_RXDV
C8	DDR_BA1	C20	GPIO1_B6/LCDC_D13/I2S_LRCLKTX/GMAC_RXD1
D6	DDR_BA2	F18	GPIO1_B5/LCDC_D14/I2S_SDIO1/GMAC_RXD0
B2	DDR_BA0	D19	GPIO1_D2/UART1_RX/SPI_RXD
B1	DDR_CS0N	A19	GPIO1_D1/UART1_RTSN/SPI_CSN0/DSP_TMS
E8	DDR_WEN	A20	GPIO1_D7/HDMI_CEC/DSP_RTCK
C9	DDR_A10	F16	GPIO2_D1/UART2_RX/JTAG_TMS
C5	DDR_ODT0	E16	GPIO2_D2/UART2_TX/JTAG_TCK
B9	DDR_CKE	C19	GPIO1_B4/LCDC_D15/I2S_MCLK/GMAC_TXEN
D8	DDR_CASN	B20	GPIO1_B3/LCDC_D16/I2S_SCLK/GMAC_TXD1
C2	DDR_CLKN	A18	GPIO1_D0/UART1_CTSN/SPI_CLK/DSP_TCK
C3	DDR_CLK	F17	GPIO1_B2/LCDC_D17/I2S_SDO/GMAC_TXD0
D5	DDR_RASN	B18	GPIO1_D3/UART1_TX/SPI_TXD/DSP_TDO
D3	DDR_DQ4	C18	5VGPIO1_D6/HDMI_HPD0
F4	DDR_DQ6	C17	5VGPIO1_D5/UART2_RTSN/HDMI_I2C0_SDA
E3	DDR_DQ7	E17	5VGPIO1_D4/UART2_CTSN/HDMI_I2C0_SCL
G2	DDR_DQ5	E15	CODEC_AVSS
K4	DDR_DQS0N	A16	CODEC_AOR
J3	DDR_DQS0	D15	CODEC_AVDD_1V8
E2	DDR_DQ1	B16	CODEC_VCM
F1	DDR_DQ3	A15	CODEC_AOL
G5	DDR_DQ2	B15	CODEC_MICR
F3	DDR_DQ0	A17	CODEC_MICBIAS
G1	DDR_DM0	C15	CODEC_MICL
L3	DDR_DM1	C14	VIDEO_AVDD_1V8
K2	DDR_DQ8	A14	VIDEO_INP
M2	DDR_DQ10	B14	VIDEO_INN

Pin #	Pin Name	Pin #	Pin Name
L2	DDR_DQ11	E14	VIDEO_AVDD_1V0
J4	DDR_DQ9	F14	APIO3_VDD
H2	DDR_DQS1	C12	GPIO3_C0/SDMMC0_D3
H3	DDR_DQS1N	D12	GPIO3_C1/SDMMC0_D2
H4	DDR_DQ13	A12	GPIO3_C2/SDMMC0_D1/UART2_RX
L1	DDR_DQ15	B12	GPIO3_C3/SDMMC0_D0/UART2_TX
L4	DDR_DQ14	B13	GPIO3_C4/SDMMC0_CLKO
K5	DDR_DQ12	A13	GPIO3_C5/SDMMC0_CMD
N3	EFUSE	D11	GPIO3_B7/SDMMC0_PWR
N6	PLL_AVDD_1V8	D13	ADC_IN0
M6	PLL_AVDD_1V0	E12	ADC_IN2
M4	GPIO0_C0/PWM3/IR	E13	ADC_IN1
M3	GPIO0_A7/SPI_TXD	D10	ADC_IN3
M5	GPIO0_B7/TSADC_SHUT	F12	ADC_IN4
R8	PMUIO_VDD	E11	ADC_IN5
N5	GPIO0_B5/PMIC_SLEEP	E4	FP_1
N1	GPIO0_B6/I2C3_SCL	F6	FP_2
P5	GPIO0_A4/SPI_CSN0	J6	DDR_VDD_1
R6	PMU_DVDD_1V0	H6	DDR_VDD_2
P1	XIN_24M	G6	DDR_VDD_3
P2	XOUT24M	E10	DDR_VDD_4
R2	GPIO0_B3	F7	DDR_VDD_5
P4	GPIO0_A3/SPI_CLK	F8	DDR_VDD_6
R3	GPIO0_C6/PWM2/I2C2_SCL/PMU_DEBUG4	F9	DDR_VDD_7
R4	GPIO0_B2/I2C0_SDA	G8	CORE_VDD_1
P7	TEST	G9	CORE_VDD_2
P6	GPIO0_C3/PMU_DEBUG2	J15	CORE_VDD_3
T4	GPIO0_B1/I2C0_SCL	G15	CORE_VDD_4
T5	GPIO0_B4	N15	CORE_VDD_5
T1	NPOR	L15	CORE_VDD_6
T2	GPIO0_C5/PWM0/PMU_DEBUG3	J7	CORE_VDD_7
T3	GPIO0_C4/PWM1/I2C3_SDA	R7	CORE_VDD_8
U1	GPIO0_A2/SDMMC1_PWR	A1	VSS_1
U5	GPIO0_B0/SPI_RXD	B19	VSS_2
U2	GPIO0_C2/I2C2_SDA/PMU_DEBUG1	W19	VSS_3
V1	GPIO0_A6/PMU_DEBUG0	K3	VSS_4
U3	GPIO0_C1/HDMI_HPD1/CVBS_CLK_IN	L7	VSS_5
V2	GPIO0_A5/CLK_WIFI_OUT	B17	VSS_6
T7	GPIO0_A1/SDMMC0_DET	G13	VSS_7
V3	HDMI_AVDD_1V8	G10	VSS_8
V5	HDMI_AVDD_1V0	R12	VSS_9
Y1	HDMI_TXCN	G14	VSS_10
W1	HDMI_TXCP	F10	VSS_11

Pin #	Pin Name	Pin #	Pin Name
W2	HDMI_TX0N	N14	VSS_12
W3	HDMI_TX0P	L5	VSS_13
W4	HDMI_TX1N	H8	VSS_14
Y4	HDMI_TX1P	H9	VSS_15
Y5	HDMI_TX2N	H10	VSS_16
W5	HDMI_TX2P	H11	VSS_17
U6	HDMI_EXTR	H12	VSS_18
U7	VDAC_AVDD_1V8	H13	VSS_19
Y6	VDAC_OUT	H14	VSS_20
W6	VDAC_EXTR	T14	VSS_21
V7	MIPI_DSI_AVDD_1V0	J8	VSS_22
U8	MIPI_DSI_AVDD_1V8	J9	VSS_23
W7	GPIO1_B1/LCDC_D9/MIPI_D3N/PWM7	J10	VSS_24
Y7	GPIO1_B0/LCDC_D8/MIPI_D3P/PWM6	J11	VSS_25
W8	GPIO1_A7/LCDC_D7/MIPI_D2N/PWM5	J12	VSS_26
U9	MIPI_DSI_AVDD_3V3	J13	VSS_27
Y8	GPIO1_A6/LCDC_D6/MIPI_D2P	L14	VSS_28
Y9	GPIO1_A0/LCDC_D4/MIPI_CLKP	K7	VSS_29
W9	GPIO1_A1/LCDC_D5/MIPI_CLKN	K8	VSS_30
W10	GPIO1_A4/LCDC_D3/MIPI_D1P	K9	VSS_31
Y10	GPIO1_A5/LCDC_D2/MIPI_D1N	K10	VSS_32
W11	GPIO1_A2/LCDC_D1/MIPI_D0P	K11	VSS_33
Y11	GPIO1_A3/LCDC_D0/MIPI_D0N	K12	VSS_34
W12	USB0_DP	K13	VSS_35
Y12	USB0_DM	K14	VSS_36
T11	USB_AVDD_3V3	G7	VSS_37
T10	USB_AVDD_1V8	L8	VSS_38
V11	USB0_ID	L9	VSS_39
U10	USB_EXTR	L10	VSS_40
T12	USB_VDD_1V0	L11	VSS_41
V12	USB_VBUS	L12	VSS_42
W13	USB1_DP	L13	VSS_43
Y13	USB1_DM	R10	VSS_44
B11	SADC_AVDD_1V8	M7	VSS_45
U12	MIPI_CSI_EXTR	M8	VSS_46
U13	MIPI_CSI_AVDD_1V0	M9	VSS_47
W14	MIPI_CSI_D0N	M10	VSS_48
Y14	MIPI_CSI_D0P	M11	VSS_49
W15	MIPI_CSI_D1N	M12	VSS_50
Y15	MIPI_CSI_D1P	M13	VSS_51
W16	MIPI_CSI_CLKP	M14	VSS_52
Y16	MIPI_CSI_CLKN	N7	VSS_53
Y17	MIPI_CSI_D2P	N8	VSS_54
W17	MIPI_CSI_D2N	N9	VSS_55

Pin #	Pin Name	Pin #	Pin Name
W18	MIPI_CSI_D3P	N10	VSS_56
Y18	MIPI_CSI_D3N	N11	VSS_57
U14	GPIO2_C1/CIF_D7/I2S_SDI	N12	VSS_58
P16	APIO5_VDD	N13	VSS_59
V14	GPIO2_C6/CIF_D3/I2S_SDIO1	D16	VSS_60
U15	GPIO2_C5/CIF_D2/I2S_MCLK	P3	VSS_61
V16	GPIO2_C3/CIF_D0/I2S_SDO	P8	VSS_62
U16	GPIO2_C4/CIF_D1/I2S_SCLK	P9	VSS_63
Y19	GPIO2_C0/CIF_D6/I2S_LRCLKRX	P10	VSS_64
U17	GPIO3_D4/CIF_D9/FLASH_TRIG_IN	P11	VSS_65
Y20	GPIO3_D3/CIF_D8/I2S_SDIO3	P12	VSS_66
V18	GPIO3_D2/CIF_CLKOUT	P13	VSS_67
T17	GPIO3_D1/CIF_PDN	P14	VSS_68
U18	GPIO3_D0/CIF_HREF	D14	VSS_69
V19	GPIO3_C6/CIF_VSYNC	M15	VSS_70
W20	GPIO3_D6/CIF_D11/PRELIGHT_TRIG_OUT	R9	VSS_71
T18	GPIO3_C7/CIF_CLKIN	C11	VSS_72
R16	GPIO3_D5/CIF_D10/FLASH_TRIG_OUT	J5	VSS_73
V20	GPIO1_C6/CIF_D4//I2S_LRCLKTX	N2	VSS_74
U19	GPIO1_C7/CIF_D5/I2S_SDIO2	R13	VSS_75
U20	GPIO3_B0	R14	VSS_76
T19	GPIO2_D3/I2C1_SDA	Y2	VSS_77
R17	GPIO2_D4/I2C1_SCL	V4	VSS_78
T16	APIO2_VDD	V6	VSS_79
P17	GPIO3_A6/UART0_TX	V8	VSS_80
T20	GPIO3_A5/UART0_RX	V10	VSS_81
R19	GPIO3_B3/PCM_CLK	V13	VSS_82
P18	GPIO3_A4/UART0_CTSN	V15	VSS_83
R20	GPIO3_A3/UART0_RTSN	V17	VSS_84
N16	GPIO3_B1/PCM_OUT/FLASH_TRIG_OUT	E1	VSS_85
P19	GPIO3_A7	G3	VSS_86
P20	GPIO3_B5/MIPI_CSI_MCLK	F2	VSS_87
N18	GPIO3_B2/PCM_IN/FLASH_TRIG_IN	D2	VSS_88
N19	GPIO3_B6	A4	VSS_89
N20	GPIO3_B4/PCM_SYNC/PRELIGHT_TRIG_OUT	C6	VSS_90
M17	GPIO3_A2/SDIO_D3	H7	VSS_91
M18	GPIO3_A0/SDIO_D1	G11	VSS_92
M19	GPIO2_D5/SDIO_CLKO	E9	VSS_93
M20	GPIO3_A1/SDIO_D2	R15	VSS_94
L20	GPIO2_D6/SDIO_CMD	A9	VSS_95
L19	GPIO2_D7/SDIO_D0	C7	VSS_96
K16	APIO6_VDD	C4	VSS_97

Pin #	Pin Name	Pin #	Pin Name
L17	GPIO2_B3/FLASH_RDN	B8	VSS_98
L16	GPIO2_A6/FLASH_D6/EMMC_D6	K1	VSS_99
K20	GPIO2_B6/EMMC_CLKO	E5	VSS_100
K19	GPIO2_B2/FLASH_WRN	R11	VSS_101
K18	GPIO2_A0/FLASH_D0/EMMC_D0/SFC_SIO_IO0	G12	VSS_102
K17	GPIO2_A2/FLASH_D2/EMMC_D2/SFC_WP_IO2	J14	VSS_103
J20	GPIO2_B5/FLASH_CSN0	M16	VSS_104
J19	GPIO2_A5/FLASH_D5/EMMC_D5	H15	VSS_105
J18	GPIO2_B7/FLASH_CSN1/SFC_CLK	K15	VSS_106
H20	GPIO2_A7/FLASH_D7/EMMC_D7		

Table 2-2 RV1108G BGA359 Pin List

Pin#	Pin Name	Pin#	Pin Name
N3	EFUSE	D11	GPIO3_B7/SDMMC0_PWR
N6	PLL_AVDD_1V8	D13	ADC_IN0
M6	PLL_AVDD_1V0	E12	ADC_IN2
M4	GPIO0_C0/PWM3/IR	E13	ADC_IN1
M3	GPIO0_A7/SPI_TXD	D10	ADC_IN3
M5	GPIO0_B7/TSADC_SHUT	F12	ADC_IN4
R8	PMUIO_VDD	E11	ADC_IN5
N5	GPIO0_B5/PMIC_SLEEP	F6	VREF
N1	GPIO0_B6/I2C3_SCL	E4	PZQ
P5	GPIO0_A4/SPI_CSN0	J6	DDR_VDD_1
R6	PMU_DVDD_1V0	H6	DDR_VDD_2
P1	XIN_24M	G6	DDR_VDD_3
P2	XOUT24M	E10	DDR_VDD_4
R2	GPIO0_B3	F7	DDR_VDD_5
P4	GPIO0_A3/SPI_CLK	F8	DDR_VDD_6
R3	GPIO0_C6/PWM2/I2C2_SCL/PMU_DEBUG4	F9	DDR_VDD_7
R4	GPIO0_B2/I2C0_SDA	H2	DDR_VDD_8
P7	TEST	H3	DDR_VDD_9
P6	GPIO0_C3/PMU_DEBUG2	H4	DDR_VDD_10
T4	GPIO0_B1/I2C0_SCL	G5	DDR_VDD_11
T5	GPIO0_B4	C2	DDR_VDD_12
T1	NPOR	C3	DDR_VDD_13
T2	GPIO0_C5/PWM0/PMU_DEBUG3	D3	DDR_VDD_14
T3	GPIO0_C4/PWM1/I2C3_SDA	A5	DDR_VDD_15
U1	GPIO0_A2/SDMMC1_PWR	B5	DDR_VDD_16
U5	GPIO0_B0/SPI_RXD	C5	DDR_VDD_17
U2	GPIO0_C2/I2C2_SDA/PMU_DEBUG1	D5	DDR_VDD_18
V1	GPIO0_A6/PMU_DEBUG0	D6	DDR_VDD_19
U3	GPIO0_C1/HDMI_HPD1/CVBS_CLK_IN	D7	DDR_VDD_20
V2	GPIO0_A5/CLK_WIFI_OUT	D8	DDR_VDD_21
T7	GPIO0_A1/SDMMC0_DET	C8	DDR_VDD_22
V3	HDMI_AVDD_1V8	A10	DDR_VDD_23
V5	HDMI_AVDD_1V0	B10	DDR_VDD_24
Y1	HDMI_TXCN	E6	DDR_VDD_25
W1	HDMI_TXCP	E7	DDR_VDD_26

Pin#	Pin Name	Pin#	Pin Name
W2	HDMI_TX0N	E8	DDR_VDD_27
W3	HDMI_TX0P	G8	CORE_VDD_1
W4	HDMI_TX1N	G9	CORE_VDD_2
Y4	HDMI_TX1P	J15	CORE_VDD_3
Y5	HDMI_TX2N	G15	CORE_VDD_4
W5	HDMI_TX2P	N15	CORE_VDD_5
U6	HDMI_EXTR	L15	CORE_VDD_6
U7	VDAC_AVDD_1V8	J7	CORE_VDD_7
Y6	VDAC_OUT	R7	CORE_VDD_8
W6	VDAC_EXTR	A1	VSS_1
V7	MIPI_DSI_AVDD_1V0	B19	VSS_2
U8	MIPI_DSI_AVDD_1V8	W19	VSS_3
W7	GPIO1_B1/LCDC_D9/MIPI_D3N/PWM7	K3	VSS_4
Y7	GPIO1_B0/LCDC_D8/MIPI_D3P/PWM6	L7	VSS_5
W8	GPIO1_A7/LCDC_D7/MIPI_D2N/PWM5	B17	VSS_6
U9	MIPI_DSI_AVDD_3V3	G13	VSS_7
Y8	GPIO1_A6/LCDC_D6/MIPI_D2P	G10	VSS_8
Y9	GPIO1_A0/LCDC_D4/MIPI_CLKP	R12	VSS_9
W9	GPIO1_A1/LCDC_D5/MIPI_CLKN	G14	VSS_10
W10	GPIO1_A4/LCDC_D3/MIPI_D1P	F10	VSS_11
Y10	GPIO1_A5/LCDC_D2/MIPI_D1N	N14	VSS_12
W11	GPIO1_A2/LCDC_D1/MIPI_D0P	L5	VSS_13
Y11	GPIO1_A3/LCDC_D0/MIPI_D0N	H8	VSS_14
W12	USB0_DP	H9	VSS_15
Y12	USB0_DM	H10	VSS_16
T11	USB_AVDD_3V3	H11	VSS_17
T10	USB_AVDD_1V8	H12	VSS_18
V11	USB0_ID	H13	VSS_19
U10	USB_EXTR	H14	VSS_20
T12	USB_VDD_1V0	T14	VSS_21
V12	USB_VBUS	J8	VSS_22
W13	USB1_DP	J9	VSS_23
Y13	USB1_DM	J10	VSS_24
B11	SADC_AVDD_1V8	J11	VSS_25
U12	MIPI_CSI_EXTR	J12	VSS_26
U13	MIPI_CSI_AVDD_1V0	J13	VSS_27
W14	MIPI_CSI_D0N	L14	VSS_28
Y14	MIPI_CSI_D0P	K7	VSS_29
W15	MIPI_CSI_D1N	K8	VSS_30
Y15	MIPI_CSI_D1P	K9	VSS_31
W16	MIPI_CSI_CLKP	K10	VSS_32
Y16	MIPI_CSI_CLKN	K11	VSS_33
Y17	MIPI_CSI_D2P	K12	VSS_34
W17	MIPI_CSI_D2N	K13	VSS_35
W18	MIPI_CSI_D3P	K14	VSS_36
Y18	MIPI_CSI_D3N	G7	VSS_37
U14	GPIO2_C1/CIF_D7/I2S_SDI	L8	VSS_38
P16	APIO5_VDD	L9	VSS_39
V14	GPIO2_C6/CIF_D3/I2S_SDIO1	L10	VSS_40
U15	GPIO2_C5/CIF_D2/I2S_MCLK	L11	VSS_41
V16	GPIO2_C3/CIF_D0/I2S_SDO	L12	VSS_42

Pin#	Pin Name	Pin#	Pin Name
U16	GPIO2_C4/CIF_D1/I2S_SCLK	L13	VSS_43
Y19	GPIO2_C0/CIF_D6/I2S_LRCLKRX	R10	VSS_44
U17	GPIO3_D4/CIF_D9/FLASH_TRIG_IN	M7	VSS_45
Y20	GPIO3_D3/CIF_D8/I2S_SDIO3	M8	VSS_46
V18	GPIO3_D2/CIF_CLKOUT	M9	VSS_47
T17	GPIO3_D1/CIF_PDN	M10	VSS_48
U18	GPIO3_D0/CIF_HREF	M11	VSS_49
V19	GPIO3_C6/CIF_VSYNC	M12	VSS_50
W20	GPIO3_D6/CIF_D11/PRELIGHT_TRIG_OUT	M13	VSS_51
T18	GPIO3_C7/CIF_CLKIN	M14	VSS_52
R16	GPIO3_D5/CIF_D10/FLASH_TRIG_OUT	N7	VSS_53
V20	GPIO1_C6/CIF_D4//I2S_LRCLKTX	N8	VSS_54
U19	GPIO1_C7/CIF_D5/I2S_SDIO2	N9	VSS_55
U20	GPIO3_B0	N10	VSS_56
T19	GPIO2_D3/I2C1_SDA	N11	VSS_57
R17	GPIO2_D4/I2C1_SCL	N12	VSS_58
T16	APIO2_VDD	N13	VSS_59
P17	GPIO3_A6/UART0_TX	D16	VSS_60
T20	GPIO3_A5/UART0_RX	P3	VSS_61
R19	GPIO3_B3/PCM_CLK	P8	VSS_62
P18	GPIO3_A4/UART0_CTSN	P9	VSS_63
R20	GPIO3_A3/UART0_RTSN	P10	VSS_64
N16	GPIO3_B1/PCM_OUT/FLASH_TRIG_OUT	P11	VSS_65
P19	GPIO3_A7	P12	VSS_66
P20	GPIO3_B5/MIPI_CSI_MCLK	P13	VSS_67
N18	GPIO3_B2/PCM_IN/FLASH_TRIG_IN	P14	VSS_68
N19	GPIO3_B6	D14	VSS_69
N20	GPIO3_B4/PCM_SYNC/PRELIGHT_TRIG_OUT	M15	VSS_70
M17	GPIO3_A2/SDIO_D3	R9	VSS_71
M18	GPIO3_A0/SDIO_D1	C11	VSS_72
M19	GPIO2_D5/SDIO_CLKO	J5	VSS_73
M20	GPIO3_A1/SDIO_D2	N2	VSS_74
L20	GPIO2_D6/SDIO_CMD	R13	VSS_75
L19	GPIO2_D7/SDIO_D0	R14	VSS_76
K16	APIO6_VDD	Y2	VSS_77
L17	GPIO2_B3/FLASH_RDN	V4	VSS_78
L16	GPIO2_A6/FLASH_D6/EMMC_D6	V6	VSS_79
K20	GPIO2_B6/EMMC_CLKO	V8	VSS_80
K19	GPIO2_B2/FLASH_WRN	V10	VSS_81
K18	GPIO2_A0/FLASH_D0/EMMC_D0/SFC_SIO_IO0	V13	VSS_82
K17	GPIO2_A2/FLASH_D2/EMMC_D2/SFC_WP_IO2	V15	VSS_83
J20	GPIO2_B5/FLASH_CSN0	V17	VSS_84
J19	GPIO2_A5/FLASH_D5/EMMC_D5	E1	VSS_85
J18	GPIO2_B7/FLASH_CSN1/SFC_CLK	G3	VSS_86
H20	GPIO2_A7/FLASH_D7/EMMC_D7	F2	VSS_87
H19	GPIO2_A3/FLASH_D3/EMMC_D3/SFC_HOLD_IO3	D2	VSS_88
J16	GPIO2_A1/FLASH_D1/EMMC_D1/SFC_SIO_IO1	A4	VSS_89
G20	GPIO2_A4/FLASH_D4/EMMC_D4	C6	VSS_90
H18	GPIO2_B0/FLASH_ALE	H7	VSS_91
G19	GPIO2_B4/FLASH_RDY/EMMC_CMD/SFC_CSN0	G11	VSS_92
F20	GPIO2_B1/FLASH_CLE	E9	VSS_93

Pin#	Pin Name	Pin#	Pin Name
H17	GPIO2_C2/FLASH_WP/EMMC_PWR	R15	VSS_94
H16	APIO1_VDD	A9	VSS_95
G17	GPIO1_C5/LCDC_CLK/GMAC_CLK	C7	VSS_96
F19	GPIO1_C4/LCDC_HSYNC/GMAC_MDC	C4	VSS_97
E20	GPIO1_C3/LCDC_VSYNC/GMAC_MDIO	B8	VSS_98
D20	GPIO1_C2/LCDC_DEN/I2S_SDIO3/GMAC_RXER	K1	VSS_99
E19	GPIO1_C1/LCDC_D10/I2S_SDI/PWM4	E5	VSS_100
E18	GPIO1_C0/LCDC_D11/I2S_LRCLKRX	R11	VSS_101
G16	GPIO1_B7/LCDC_D12/I2S_SDIO2/GMAC_RXDV	G12	VSS_102
C20	GPIO1_B6/LCDC_D13/I2S_LRCLKTX/GMAC_RXD1	J14	VSS_103
F18	GPIO1_B5/LCDC_D14/I2S_SDIO1/GMAC_RXD0	M16	VSS_104
D19	GPIO1_D2/UART1_RX/SPI_RXD	H15	VSS_105
A19	GPIO1_D1/UART1_RTSN/SPI_CSN0/DSP_TMS	K15	VSS_106
A20	GPIO1_D7/HDMI_CEC/DSP_RTCK	A2	VSS_107
F16	GPIO2_D1/UART2_RX/JTAG_TMS	A3	VSS_108
E16	GPIO2_D2/UART2_TX/JTAG_TCK	B1	VSS_109
C19	GPIO1_B4/LCDC_D15/I2S_MCLK/GMAC_TXEN	B2	VSS_110
B20	GPIO1_B3/LCDC_D16/I2S_SCLK/GMAC_TXD1	B3	VSS_111
A18	GPIO1_D0/UART1_CTSN/SPI_CLK/DSP_TCK	B4	VSS_112
F17	GPIO1_B2/LCDC_D17/I2S_SDO/GMAC_TXD0	B6	VSS_113
B18	GPIO1_D3/UART1_TX/SPI_TXD/DSP_TDO	B7	VSS_114
C18	5VGPIO1_D6/HDMI_HPD0	A6	VSS_115
C17	5VGPIO1_D5/UART2_RTSN/HDMI_I2C0_SDA	B9	VSS_116
E17	5VGPIO1_D4/UART2_CTSN/HDMI_I2C0_SCL	C9	VSS_117
E15	CODEC_AVSS	G1	VSS_118
A16	CODEC_AOR	G2	VSS_119
D15	CODEC_AVDD_1V8	L4	VSS_120
B16	CODEC_VCM	F1	VSS_121
A15	CODEC_AOL	E2	VSS_122
B15	CODEC_MICR	E3	VSS_123
A17	CODEC_MICBIAS	F3	VSS_124
C15	CODEC_MICL	F4	VSS_125
C14	VIDEO_AVDD_1V8	F5	VSS_126
A14	VIDEO_INP	J3	VSS_127
B14	VIDEO_INN	J4	VSS_128
E14	VIDEO_AVDD_1V0	K2	VSS_129
F14	APIO3_VDD	K4	VSS_130
C12	GPIO3_C0/SDMMC0_D3	L1	VSS_131
D12	GPIO3_C1/SDMMC0_D2	L2	VSS_132
A12	GPIO3_C2/SDMMC0_D1/UART2_RX	L3	VSS_133
B12	GPIO3_C3/SDMMC0_D0/UART2_TX	M2	VSS_134
B13	GPIO3_C4/SDMMC0_CLKO	K5	VSS_135
A13	GPIO3_C5/SDMMC0_CMD		

2.6 RV1108 Power/ground Pin Descriptions

Table 2-3 RV1108A Power/Ground Pin Description

Group	Ball#	Descriptions
GND	A1,A4,A9 B8,B17,B19 C4,C6,C7,C11 D2,D14,D16 E1,E5,E9, F2,F10 G3,G7,G10,G11,G12,G13,G14 H7,H8,H9,H10,H11,H12,H13,H14,H15 J5,J8,J9,J10,J11,J12,J13,J14 K1,K3,K7,K8,K9,K10,K11,K12,K13,K14,K15 L5,L7,L8,L9,L10,L11,L12,L13,L14 M7,M8,M9,M10,M11,M12,M13,M14,M15,M16 N2,N7,N8,N9,N10,N11,N12,N13,N14 P3,P8,P9,P10,P11,P12,P13,P14 R9,R10,R11,R12,R13,R14,R15 T14,V4,V6,V8,V10,V13,V15,V17,W19,Y2	Internal Core Ground Digital IO Ground
CODEC_AVSS	E15	Analog Codec Ground
PLL_AVDD_1V8	N6	PLL IO Power
PLL_AVDD_1V0	M6	General PLL Analog Power
CORE_VDD	G8,G9,J15,G15,N15,L15,J7,R7	ARM Core Power
PMU_DVDD_1V0	R6	PMU IO Domain(PowerDomain) Power
PMUIO_VDD	R8	PMU IO Power
APIO1_VDD	H16	APIO1 PowerDomain Power
APIO2_VDD	T16	APIO2 PowerDomain Power
APIO3_VDD	F14	APIO3 PowerDomain Power
APIO5_VDD	P16	APIO5 PowerDomain Power
APIO6_VDD	K16	APIO6 PowerDomain Power
DDR_VDD	J6,H6,G6,E10,F7,F8,F9	DDR PHY Power
USB_VDD_1V0	T12	USB OTG2.0/Host2.0 Digital Power
USB_AVDD_1V8	T10	USB OTG2.0/Host2.0 Analog Power
USB_AVDD_3V3	T11	USB OTG2.0/Host2.0 Analog Power
MIPI_CSI_AVDD_1V0	U13	MIPI_CSI PHY Analog Power
MIPI_DSI_AVDD_1V0	V7	MIPI_DSI PHY Analog Power
MIPI_DSI_AVDD_1V8	U8	MIPI_DSI PHY Analog Power
MIPI_DSI _AVDD_3V3	U9	MIPI_DSI PHY Analog Power
HDMI_AVDD_1V8	V3	HDMI PHY Analog Power
HDMI_AVDD_1V0	V5	HDMI PHY Analog Power
SADC_AVDD_1V8	B11	SADC Analog Power
CODEC_AVDD_1V8	D15	Audio Codec Analog Power
VDAC_AVDD_1V8	U7	VDAC Analog Power
VIDEO_AVDD_1V0	E14	VIDEO Analog Power
VIDEO_AVDD_1V8	C14	VIDEO Analog Power

Table 2-4 RV1108G Power/Ground IO information

Group	Ball#	Descriptions
GND	A1,A2,A3,A4,A6,A9 B1,B2,B3,B4,B6,B7,B8,B9,B17,B19 C4,C6,C7,C9,C11 D2,D14,D16 E1,E2,E3,E4,E5,E9,E10 F1,F2,F3,F4,F5,F6,F10 G1,G2,G3,G7,G10,G11,G12,G13,G14 H7,H8,H9,H10,H11,H12,H13,H14,H15 J3,J4,J5,J8,J9,J10,J11,J12,J13,J14 K1,K2,K3,K4,K5,K7,K8,K9,K10,K11,K12,K13,K14,K15 L1,L2,L3,L4,L5,L7,L8,L9,L10,L11,L12,L13,L14 M2,M7,M8,M9,M10,M11,M12,M13,M14,M15,M16 N2,N7,N8,N9,N10,N11,N12,N13,N14 P3,P8,P9,P10,P11,P12,P13,P14 R9,R10,R11,R12,R13,R14,R15 T14,V4,V6,V8,V10,V13,V15,V17,W19,Y2	Internal Core Ground Digital IO Ground
CODEC_AVSS	E15	Analog Codec Ground
PLL_AVDD_1V8	N6	PLL IO Power
PLL_AVDD_1V0	M6	General PLL Analog Power
CORE_VDD	G8,G9,J15,G15,N15,L15,J7,R7	ARM Core Power
PMU_DVDD_1V0	R6	PMU IO Domain(PowerDomain) Power
PMUIO_VDD	R8	PMU IO Power
APIO1_VDD	H16	APIO1 PowerDomain Power
APIO2_VDD	T16	APIO2 PowerDomain Power
APIO3_VDD	F14	APIO3 PowerDomain Power
APIO5_VDD	P16	APIO5 PowerDomain Power
APIO6_VDD	K16	APIO6 PowerDomain Power
DDR_VDD	A5,A10,B5,B10,C2,C3,C5,C8,D3,D6,D7,D8,E6,E7,G5,J6,H6,G6,E10,F7,F8,F9,H2,H3,H4	DDR PHY Power
USB_VDD_1V0	T12	USB OTG2.0/Host2.0 Digital Power
USB_AVDD_1V8	T10	USB OTG2.0/Host2.0 Analog Power
USB_AVDD_3V3	T11	USB OTG2.0/Host2.0 Analog Power
MIPI_CSI_AVDD_1V0	U13	MIPI_CSI PHY Analog Power
MIPI_DSI_AVDD_1V0	V7	MIPI_DSI PHY Analog Power
MIPI_DSI_AVDD_1V8	U8	MIPI_DSI PHY Analog Power
MIPI_DSI_AVDD_3V3	U9	MIPI_DSI PHY Analog Power
HDMI_AVDD_1V8	V3	HDMI PHY Analog Power
HDMI_AVDD_1V0	V5	HDMI PHY Analog Power
SADC_AVDD_1V8	B11	SADC Analog Power
CODEC_AVDD_1V8	D15	Audio Codec Analog Power
VDAC_AVDD_1V8	U7	VDAC Analog Power
VIDEO_AVDD_1V0	E14	VIDEO Analog Power
VIDEO_AVDD_1V8	C14	VIDEO Analog Power

2.7 RV1108 Pin Description

Table 2-5 RV1108A Pin Description

Pin	Pin Name	Func1	Func2	Func3	Func4	Pad Type①	Def®	Pull	Drive Strength®	INT®	DIE Power domain
T7	GPIO0_A1/SDMMC0_DET	GPIO0_A1	SDMMC0_DET			I/O	I	up	4	√	
U1	GPIO0_A2/SDMMC1_PWR	GPIO0_A2	SDMMC1_PWR			I/O	I	down	4	√	
P4	GPIO0_A3/SPI_CLK	GPIO0_A3	SPI_CLK			I/O	I	down	4	√	
P5	GPIO0_A4/SPI_CSN0	GPIO0_A4	SPI_CSN0			I/O	I	down	4	√	
V2	GPIO0_A5/CLK_WIFI_OUT	GPIO0_A5	CLK_WIFI_OUT			I/O	I	up	4	√	
V1	GPIO0_A6/PMU_DEBUG0	GPIO0_A6	PMU_DEBUG0			I/O	I	down	4	√	
M3	GPIO0_A7/SPI_TXD	GPIO0_A7	SPI_TXD			I/O	I	down	4	√	
U5	GPIO0_B0/SPI_RXD	GPIO0_B0	SPI_RXD			I/O	I	down	4	√	
T4	GPIO0_B1/I2C0_SCL	GPIO0_B1	I2C0_SCL			I/O	I	up	4	√	
R4	GPIO0_B2/I2C0_SDA	GPIO0_B2	I2C0_SDA			I/O	I	up	4	√	
R2	GPIO0_B3	GPIO0_B3				I/O	I	up	4	√	
T5	GPIO0_B4	GPIO0_B4				I/O	I	up	4	√	
N5	GPIO0_B5/PMIC_SLEEP	GPIO0_B5	PMIC_SLEEP			I/O	I	down	4	√	PMUIO
N1	GPIO0_B6/I2C3_SCL	GPIO0_B6	I2C3_SCL			I/O	I	up	4	√	IO Voltage
M5	GPIO0_B7/TSADC_SHUT	GPIO0_B7	TSADC_SHUT			I/O	I	up	4	√	3.3V
M4	GPIO0_C0/PWM3/IR	GPIO0_C0	PWM3	IR		I/O	I	down	4	√	
U3	GPIO0_C1/HDMI_HPD1/CVBS_CLK_IN	GPIO0_C1	HDMI_HPD1	CVBS_CLK_IN		I/O	I	down	4	√	
U2	GPIO0_C2/I2C2_SDA/PMU_DEBUG1	GPIO0_C2	I2C4_SDA	PMU_DEBUG1		I/O	I	down	4	√	
P6	GPIO0_C3/PMU_DEBUG2	GPIO0_C3	PMU_DEBUG2			I/O	I	down	4	√	
T3	GPIO0_C4/PWM1/I2C3_SDA	GPIO0_C4	PWM1	I2C3_SDA		I/O	I	up	4	√	
T2	GPIO0_C5/PWM0/PMU_DEBUG3	GPIO0_C5	PWM0	PMU_DEBUG3		I/O	I	down	4	√	
R3	GPIO0_C6/PWM2/I2C2_SCL/PMU_DEBUG4	GPIO0_C6	PWM2	I2C4_SCL	PMU_DEBUG4	I/O	I	down	4	√	
Y9	GPIO1_A0/LCDC_D4/MIPI_CLKP	GPIO1_A0	LCDC_D4	MIPI_CLKP		A		NA		√	
W9	GPIO1_A1/LCDC_D5/MIPI_CLKN	GPIO1_A1	LCDC_D5	MIPI_CLKN		A		NA		√	
W11	GPIO1_A2/LCDC_D1/MIPI_D0P	GPIO1_A2	LCDC_D1	MIPI_D0P	4	A		NA		√	
Y11	GPIO1_A3/LCDC_D0/MIPI_D0N	GPIO1_A3	LCDC_D0	MIPI_D0N		A		NA		√	
W10	GPIO1_A4/LCDC_D3/MIPI_D1P	GPIO1_A4	LCDC_D3	MIPI_D1P		A		NA		√	
Y10	GPIO1_A5/LCDC_D2/MIPI_D1N	GPIO1_A5	LCDC_D2	MIPI_D1N		A		NA		√	MIPI_DSI
Y8	GPIO1_A6/LCDC_D6/MIPI_D2P	GPIO1_A6	LCDC_D6	MIPI_D2P		A		NA		√	
W8	GPIO1_A7/LCDC_D7/MIPI_D2N/PWM5	GPIO1_A7	LCDC_D7	MIPI_D2N	PWM5	A		NA		√	
Y7	GPIO1_B0/LCDC_D8/MIPI_D3P/PWM6	GPIO1_B0	LCDC_D8	MIPI_D3P	PWM6	A		NA		√	
W7	GPIO1_B1/LCDC_D9/MIPI_D3N/PWM7	GPIO1_B1	LCDC_D9	MIPI_D3N	PWM7	A		NA		√	
F17	GPIO1_B2/LCDC_D17/I2S_SDO/GMAC_TXD0	GPIO1_B2	LCDC_D17	I2S_SDO	GMAC_TXD0	I/O	I	down	8	√	
B20	GPIO1_B3/LCDC_D16/I2S_SCLK/GMAC_TXD1	GPIO1_B3	LCDC_D16	I2S_SCLK	GMAC_TXD1	I/O	I	down	8	√	
C19	GPIO1_B4/LCDC_D15/I2S_MCLK/GMAC_TXEN	GPIO1_B4	LCDC_D15	I2S_MCLK	GMAC_TXEN	I/O	I	down	8	√	
F18	GPIO1_B5/LCDC_D14/I2S_SDIO1/GMAC_RXD0	GPIO1_B5	LCDC_D14	I2S_SDIO1	GMAC_RXD0	I/O	I	down	8	√	
C20	GPIO1_B6/LCDC_D13/I2S_LRCLKTX/GMAC_RXD1	GPIO1_B6	LCDC_D13	I2S_LRCLKTX	GMAC_RXD1	I/O	I	down	8	√	APIO1
G16	GPIO1_B7/LCDC_D12/I2S_SDIO2/GMAC_RXDV	GPIO1_B7	LCDC_D12	I2S_SDIO2	GMAC_RXDV	I/O	I	down	8	√	IO Voltage
E18	GPIO1_C0/LCDC_D11/I2S_LRCLKRX	GPIO1_C0	LCDC_D11	I2S_LRCLKRX		I/O	I	down	8	√	3.3V/1.8V
E19	GPIO1_C1/LCDC_D10/I2S_SDI/PWM4	GPIO1_C1	LCDC_D10	I2S_SDI	PWM4	I/O	I	down	8	√	
D20	GPIO1_C2/LCDC_DEN/I2S_SDIO3/GMAC_RXER	GPIO1_C2	LCDC_DEN	I2S_SDIO3	GMAC_RXER	I/O	I	down	8	√	

Pin	Pin Name	Func1	Func2	Func3	Func4	Pad Type①	Def®	Pull	Drive Strength®	INT®	DIE Power domain
E20	GPIO1_C3/LCDC_VSYNC/GMAC_MDIO	GPIO1_C3	LCDC_VSYNC	GMAC_MDIO		I/O	I	down	8	√	
F19	GPIO1_C4/LCDC_HSYNC/GMAC_MDC	GPIO1_C4	LCDC_HSYNC	GMAC_MDC		I/O	I	down	8	√	
G17	GPIO1_C5/LCDC_CLK/GMAC_CLK	GPIO1_C5	LCDC_CLK	GMAC_CLK		I/O	I	down	8	√	
A18	GPIO1_D0/UART1_CTSN/SPI_CLK/DSP_TCK	GPIO1_D0	UART1_CTSN	SPI_CLK	DSP_TCK	I/O	I	down	4	√	
A19	GPIO1_D1/UART1_RTSN/SPI_CSN0/DSP_TMS	GPIO1_D1	UART1_RTSN	SPI_CSN0	DSP_TMS	I/O	I	up	4	√	
D19	GPIO1_D2/UART1_RX/SPI_RXD	GPIO1_D2	UART1_RX	SPI_RXD		I/O	I	up	4	√	
B18	GPIO1_D3/UART1_TX/SPI_TXD/DSP_TDO	GPIO1_D3	UART1_TX	SPI_TXD	DSP_TDO	I/O	I	down	4	√	
E17	5VGPIO1_D4/UART2_CTSN/HDMI_I2C0_SCL	5VGPIO1_D4	UART2_CTSN	HDMI_I2C0_SCL		I/O	I	up	4	√	
C17	5VGPIO1_D5/UART2_RTSN/HDMI_I2C0_SDA	5VGPIO1_D5	UART2_RTSN	HDMI_I2C0_SDA		I/O	I	up	4	√	
C18	5VGPIO1_D6/HDMI_HPD0	5VGPIO1_D6	HDMI_HPD0			I/O	I	down	4	√	
A20	GPIO1_D7/HDMI_CEC/DSP_RTCK	GPIO1_D7	HDMI_CEC	DSP_RTCK		I/O	I	up	4	√	
F16	GPIO2_D1/UART2_RX/JTAG_TMS	GPIO2_D1	UART2_RX	JTAG_TMS		I/O	I	up	4	√	
E16	GPIO2_D2/UART2_TX/JTAG_TCK	GPIO2_D2	UART2_TX	JTAG_TCK		I/O	I	up	4	√	
T19	GPIO2_D3/I2C1_SDA	GPIO2_D3	I2C1_SDA			I/O	I	up	4	√	
R17	GPIO2_D4/I2C1_SCL	GPIO2_D4	I2C1_SCL			I/O	I	up	4	√	
M19	GPIO2_D5/SDIO_CLKO	GPIO2_D5	SDIO_CLKO			I/O	I	down	4	√	
L20	GPIO2_D6/SDIO_CMD	GPIO2_D6	SDIO_CMD			I/O	I	up	8	√	
L19	GPIO2_D7/SDIO_D0	GPIO2_D7	SDIO_D0			I/O	I	up	8	√	
M18	GPIO3_A0/SDIO_D1	GPIO3_A0	SDIO_D1			I/O	I	up	8	√	
M20	GPIO3_A1/SDIO_D2	GPIO3_A1	SDIO_D2			I/O	I	up	8	√	
M17	GPIO3_A2/SDIO_D3	GPIO3_A2	SDIO_D3			I/O	I	up	8	√	
R20	GPIO3_A3/UART0_RTSN	GPIO3_A3	UART0_RTSN			I/O	I	up	4	√	
P18	GPIO3_A4/UART0_CTSN	GPIO3_A4	UART0_CTSN			I/O	I	up	4	√	
T20	GPIO3_A5/UART0_RX	GPIO3_A5	UART0_RX			I/O	I	up	4	√	APIO2
P17	GPIO3_A6/UART0_TX	GPIO3_A6	UART0_TX			I/O	I	up	4	√	IO Vlotage
P19	GPIO3_A7	GPIO3_A7				I/O	I	down	4	√	3.3V/1.8V
U20	GPIO3_B0	GPIO3_B0				I/O	I	down	4	√	
N16	GPIO3_B1/PCM_OUT/FLASH_TRIG_OUT	GPIO3_B1	PCM_OUT	FLASH_TRIG_OUT		I/O	I	down	4	√	
N18	GPIO3_B2/PCM_IN/FLASH_TRIG_IN	GPIO3_B2	PCM_IN	FLASH_TRIG_IN		I/O	I	down	4	√	
R19	GPIO3_B3/PCM_CLK	GPIO3_B3	PCM_CLK			I/O	I	down	4	√	
N20	GPIO3_B4/PCM_SYNC/PRELIGHT_TRIG_OUT	GPIO3_B4	PCM_SYNC	PRELIGHT_TRIG_OUT		I/O	I	down	4	√	
P20	GPIO3_B5/MIPI_CSI_MCLK	GPIO3_B5	MIPI_CSI_MCLK			I/O	I	down	4	√	
N19	GPIO3_B6	GPIO3_B6				I/O	I	down	4	√	
D11	GPIO3_B7/SDMMC0_PWR	GPIO3_B7	SDMMC0_PWR			I/O	I	down	8	√	
C12	GPIO3_C0/SDMMC0_D3	GPIO3_C0	SDMMC0_D3			I/O	I	up	8	√	
D12	GPIO3_C1/SDMMC0_D2	GPIO3_C1	SDMMC0_D2	UART2_RX		I/O	I	up	8	√	APIO3
A12	GPIO3_C2/SDMMC0_D1/UART2_RX	GPIO3_C2	SDMMC0_D1	UART2_TX		I/O	I	up	8	√	IO Voltage
B12	GPIO3_C3/SDMMC0_D0/UART2_TX	GPIO3_C3	SDMMC0_D0			I/O	I	up	8	√	3.3V/1.8V
B13	GPIO3_C4/SDMMC0_CLKO	GPIO3_C4	SDMMC0_CLKO			I/O	I	up	8	√	
A13	GPIO3_C5/SDMMC0_CMD	GPIO3_C5	SDMMC0_CMD			I/O	I	down	4	√	
V20	GPIO1_C6/CIF_D4/I2S_LRCLKTX	GPIO1_C6	CIF_D4	I2S_LRCLKTX		I/O	I	down	8	√	
U19	GPIO1_C7/CIF_D5/I2S_SDIO2	GPIO1_C7	CIF_D5	I2S_SDIO2		I/O	I	down	8	√	
Y19	GPIO2_C0/CIF_D6/I2S_LRCLKRX	GPIO2_C0	CIF_D6	I2S_LRCLKRX		I/O	I	down	8	√	APIO5
U14	GPIO2_C1/CIF_D7/I2S_SDI	GPIO2_C1	CIF_D7	I2S_SDI		I/O	I	down	8	√	IO Voltage
V16	GPIO2_C3/CIF_D0/I2S_SDO	GPIO2_C3	CIF_D0	I2S_SDO		I/O	I	down	8	√	3.3V/1.8V
U16	GPIO2_C4/CIF_D1/I2S_SCLK	GPIO2_C4	CIF_D1	I2S_SCLK		I/O	I	down	8	√	

Pin	Pin Name	Func1	Func2	Func3	Func4	Pad Type①	Def®	Pull	Drive Strength®	INT®	DIE Power domain
U15	GPIO2_C5/CIF_D2/I2S_MCLK	GPIO2_C5	CIF_D2	I2S_MCLK		I/O	I	down	8	√	
V14	GPIO2_C6/CIF_D3/I2S_SDIO1	GPIO2_C6	CIF_D3	I2S_SDIO1		I/O	I	down	8	√	
V19	GPIO3_C6/CIF_VSYNC	GPIO3_C6	CIF_VSYNC			I/O	I	down	8	√	
T18	GPIO3_C7/CIF_CLKIN	GPIO3_C7	CIF_CLKIN			I/O	I	down	8	√	
U18	GPIO3_D0/CIF_HREF	GPIO3_D0	CIF_HREF			I/O	I	down	8	√	
T17	GPIO3_D1/CIF_PDN	GPIO3_D1	TCIF_PDN			I/O	I	down	8	√	
V18	GPIO3_D2/CIF_CLKOUT	GPIO3_D2	CIF_CLKOUT			I/O	I	down	8	√	
Y20	GPIO3_D3/CIF_D8/I2S_SDIO3	GPIO3_D3	CIF_D8	I2S_SDIO3		I/O	I	down	8	√	
U17	GPIO3_D4/CIF_D9/FLASH_TRIG_IN	GPIO3_D4	CIF_D9	FLASH_TRIG_IN		I/O	I	down	8	√	
R16	GPIO3_D5/CIF_D10/FLASH_TRIG_OUT	GPIO3_D5	CIF_D10	FLASH_TRIG_OUT		I/O	I	down	8	√	
W20	GPIO3_D6/CIF_D11/PRELIGHT_TRIG_OUT	GPIO3_D6	CIF_D11	PRELIGHT_TRIG_OUT		I/O	I	down	8	√	
K18	GPIO2_A0/FLASH_D0/EMMC_D0/SFC_SIO_IO0	GPIO2_A0	FLASH_D0	EMMC_D0	SFC_SIO_IO0	I/O	I	up	8	√	APIO6 IO Voltage 3.3V/1.8V
J16	GPIO2_A1/FLASH_D1/EMMC_D1/SFC_SIO_IO1	GPIO2_A1	FLASH_D1	EMMC_D1	SFC_SIO_IO1	I/O	I	up	8	√	
K17	GPIO2_A2/FLASH_D2/EMMC_D2/SFC_WP_IO2	GPIO2_A2	FLASH_D2	EMMC_D2	SFC_WP_IO2	I/O	I	up	8	√	
H19	GPIO2_A3/FLASH_D3/EMMC_D3/SFC_HOLD_IO3	GPIO2_A3	FLASH_D3	EMMC_D3	SFC_HOLD_IO3	I/O	I	up	8	√	
G20	GPIO2_A4/FLASH_D4/EMMC_D4	GPIO2_A4	FLASH_D4	EMMC_D4		I/O	I	up	8	√	
J19	GPIO2_A5/FLASH_D5/EMMC_D5	GPIO2_A5	FLASH_D5	EMMC_D5		I/O	I	up	8	√	
L16	GPIO2_A6/FLASH_D6/EMMC_D6	GPIO2_A6	FLASH_D6	EMMC_D6		I/O	I	up	8	√	
H20	GPIO2_A7/FLASH_D7/EMMC_D7	GPIO2_A7	FLASH_D7	EMMC_D7		I/O	I	up	8	√	
H18	GPIO2_B0/FLASH_ALE	GPIO2_B0	FLASH_ALE			I/O	I	down	8	√	
F20	GPIO2_B1/FLASH_CLE	GPIO2_B1	FLASH_CLE			I/O	I	down	8	√	
K19	GPIO2_B2/FLASH_WRN	GPIO2_B2	FLASH_WRN			I/O	I	up	8	√	
L17	GPIO2_B3/FLASH_RDN	GPIO2_B3	FLASH_RDN			I/O	I	up	8	√	
G19	GPIO2_B4/FLASH_RDY/EMMC_CMD/SFC_CSN0	GPIO2_B4	FLASH_RDY	EMMC_CMD	SFC_CSN0	I/O	I	up	8	√	
J20	GPIO2_B5/FLASH_CSN0	GPIO2_B5	FLASH_CSN0			I/O	I	up	8	√	
K20	GPIO2_B6/EMMC_CLKO	GPIO2_B6	EMMC_CLKO			I/O	I	down	8	√	
J18	GPIO2_B7/FLASH_CSN1/SFC_CLK	GPIO2_B7	FLASH_CSN1	SFC_CLK		I/O	I	up	8	√	
H17	GPIO2_C2/FLASH_WP/EMMC_PWR	GPIO2_C2	FLASH_WP	EMMC_PWR		I/O	I	down	8	√	
W14	MIPI_CSI_D0N	MIPI_CSI_D0N				A		NA			MIPI_CSI
Y14	MIPI_CSI_D0P	MIPI_CSI_D0P				A		NA			
W15	MIPI_CSI_D1N	MIPI_CSI_D1N				A		NA			
Y15	MIPI_CSI_D1P	MIPI_CSI_D1P				A		NA			
W17	MIPI_CSI_D2N	MIPI_CSI_D2N				A		NA			
Y17	MIPI_CSI_D2P	MIPI_CSI_D2P				A		NA			
Y18	MIPI_CSI_D3N	MIPI_CSI_D3N				A		NA			
W18	MIPI_CSI_D3P	MIPI_CSI_D3P				A		NA			
W16	MIPI_CSI_CLKP	MIPI_CSI_CLKP				A		NA			
Y16	MIPI_CSI_CLKN	MIPI_CSI_CLKN				A		NA			
U12	MIPI_CSI_EXTR	MIPI_CSI_EXTR				A		NA			
P7	TEST	TEST				I		down			PMUIO 3.3V
T1	NPOR	NPOR				I		up			
P2	XOUT_24M	XOUT_24M				O		NA			PLL_1V0
P1	XIN_24M	XIN_24M				I		NA			
Y1	HDMI_TXCN	HDMI_TXCN				A		NA			HDMI
W1	HDMI_TXCP	HDMI_TXCP				A		NA			
W2	HDMI_TX0N	HDMI_TX0N				A		NA			
W3	HDMI_TX0P	HDMI_TX0P				A		NA			
W4	HDMI_TX1N	HDMI_TX1N				A		NA			
Y4	HDMI_TX1P	HDMI_TX1P				A		NA			

Pin	Pin Name	Func1	Func2	Func3	Func4	Pad Type①	Def®	Pull	Drive Strength®	INT®	DIE Power domain
Y5	HDMI_TX2N	HDMI_TX2N				A		NA			
W5	HDMI_TX2P	HDMI_TX2P				A		NA			
U6	HDMI_EXTR	HDMI_EXTR				A		NA			
W13	USB1_DP	USB1_DP				A		NA			
Y13	USB1_DM	USB1_DM				A		NA			
U10	USB_EXTR	USB_EXTR				A		NA			
V12	USB_VBUS	USB_VBUS				A		NA			USB
V11	USB0_ID	USB0_ID				A		NA			
Y12	USB0_DM	USB0_DM				A		NA			
W12	USB0_DP	USB0_DP				A		NA			
A17	CODEC_MICBIAS	CODEC_MICBIAS				A		NA			
C15	CODEC_MICL	CODEC_MICL				A		NA			
B15	CODEC_MICR	CODEC_MICR				A		NA			
B16	CODEC_VCM	CODEC_VCM				A		NA			Audio Codec
A15	CODEC_AOL	CODEC_AOL				A		NA			
A16	CODEC_AOR	CODEC_AOR				A		NA			
A14	VIDEO_IN_P	VIDEO_IN_P				A		NA			
B14	VIDEO_IN_N	VIDEO_IN_N				A		NA			VADC_AVDD
W6	VDAC_EXTR	VDAC_EXTR				P		NA			
Y6	VDAC_OUT	VDAC_OUT				A		NA			VDAC_AVDD
D13	ADC_IN0	ADC_IN0				A		NA			
E13	ADC_IN1	ADC_IN1				A		NA			
E12	ADC_IN2	ADC_IN2				A		NA			
D10	ADC_IN3	ADC_IN3				A		NA			SAR_AVDD_18
F12	ADC_IN4	ADC_IN4				A		NA			
E11	ADC_IN5	ADC_IN5				A		NA			
N3	EFUSE	EFUSE				P		NA			EFUSE
F3	DDR_DQ0	DDR_DQ0				A		NA			
E2	DDR_DQ1	DDR_DQ1				A		NA			
G5	DDR_DQ2	DDR_DQ2				A		NA			
F1	DDR_DQ3	DDR_DQ3				A		NA			
D3	DDR_DQ4	DDR_DQ4				A		NA			
G2	DDR_DQ5	DDR_DQ5				A		NA			
F4	DDR_DQ6	DDR_DQ6				A		NA			
E3	DDR_DQ7	DDR_DQ7				A		NA			
K2	DDR_DQ8	DDR_DQ8				A		NA			
J4	DDR_DQ9	DDR_DQ9				A		NA			
M2	DDR_DQ10	DDR_DQ10				A		NA			
L2	DDR_DQ11	DDR_DQ11				A		NA			
K5	DDR_DQ12	DDR_DQ12				A		NA			
H4	DDR_DQ13	DDR_DQ13				A		NA			
L4	DDR_DQ14	DDR_DQ14				A		NA			
L1	DDR_DQ15	DDR_DQ15				A		NA			
J3	DDR_DQS0	DDR_DQS0				A		NA			
K4	DDR_DQS0n	DDR_DQS0n				A		NA			
H2	DDR_DQS1	DDR_DQS1				A		NA			
H3	DDR_DQS1n	DDR_DQS1n				A		NA			
G1	DDR_DM0	DDR_DM0				A		NA			DDR_VDD
L3	DDR_DM1	DDR_DM1				A		NA			
E4	PZQ	PZQ				A		NA			
F6	VREF	VREF				A		NA			
B4	DDR_A0	DDR_A0				A		NA			
B10	DDR_A1	DDR_A1				A		NA			
A3	DDR_A2	DDR_A2				A		NA			
E6	DDR_A3	DDR_A3				A		NA			
B6	DDR_A4	DDR_A4				A		NA			

Pin	Pin Name	Func1	Func2	Func3	Func4	Pad Type①	Def®	Pull	Drive Strength®	INT®	DIE Power domain
B3	DDR_A5	DDR_A5				A		NA			
A6	DDR_A6	DDR_A6				A		NA			
A2	DDR_A7	DDR_A7				A		NA			
A10	DDR_A8	DDR_A8				A		NA			
E7	DDR_A9	DDR_A9				A		NA			
C9	DDR_A10	DDR_A10				A		NA			
B5	DDR_A11	DDR_A11				A		NA			
B7	DDR_A12	DDR_A12				A		NA			
D7	DDR_A13	DDR_A13				A		NA			
A5	DDR_A14	DDR_A14				A		NA			
C3	DDR_CLK	DDR_CLK				A		NA			
C2	DDR_CLKn	DDR_CLKn				A		NA			
B2	DDR_BA0	DDR_BA0				A		NA			
C8	DDR_BA1	DDR_BA1				A		NA			
D6	DDR_BA2	DDR_BA2				A		NA			
C5	DDR_ODT0	DDR_ODT0				A		NA			
B1	DDR_CSN	DDR_CSN				A		NA			
B9	DDR_CKE	DDR_CKE				A		NA			
D5	DDR_RASN	DDR_RASN				A		NA			
D8	DDR_CASN	DDR_CASN				A		NA			
E8	DDR_WEN	DDR_WEN				A		NA			
F5	DDR_RESET	DDR_RESET				A		NA			
J6	DDR_VDD_1	DDR_VDD_1				A		NA			
H6	DDR_VDD_2	DDR_VDD_2				A		NA			
G6	DDR_VDD_3	DDR_VDD_3				A		NA			
E10	DDR_VDD_4	DDR_VDD_4				A		NA			
F7	DDR_VDD_5	DDR_VDD_5				A		NA			
F8	DDR_VDD_6	DDR_VDD_6				A		NA			
F9	DDR_VDD_7	DDR_VDD_7				A		NA			

Table 2-6 RV1108G Pin Description

Pin	Pin Name	Func1	Func2	Func3	Func4	Pad Type①	Def®	Pull	Drive Strength®	INT®	DIE Power domain
T7	GPIO0_A1/SDMMC0_DET	GPIO0_A1	SDMMC0_DET			I/O	I	up	4	√	
U1	GPIO0_A2/SDMMC1_PWR	GPIO0_A2	SDMMC1_PWR			I/O	I	down	4	√	
P4	GPIO0_A3/SPI_CLK	GPIO0_A3	SPI_CLK			I/O	I	down	4	√	
P5	GPIO0_A4/SPI_CSN0	GPIO0_A4	SPI_CSN0			I/O	I	down	4	√	
V2	GPIO0_A5/CLK_WIFI_OUT	GPIO0_A5	CLK_WIFI_OUT			I/O	I	up	4	√	
V1	GPIO0_A6/PMU_DEBUG0	GPIO0_A6	PMU_DEBUG0			I/O	I	down	4	√	PMUIO IO Voltage 3.3V
M3	GPIO0_A7/SPI_TXD	GPIO0_A7	SPI_TXD			I/O	I	down	4	√	
U5	GPIO0_B0/SPI_RXD	GPIO0_B0	SPI_RXD			I/O	I	down	4	√	
T4	GPIO0_B1/I2C0_SCL	GPIO0_B1	I2C0_SCL			I/O	I	up	4	√	
R4	GPIO0_B2/I2C0_SDA	GPIO0_B2	I2C0_SDA			I/O	I	up	4	√	
R2	GPIO0_B3	GPIO0_B3				I/O	I	up	4	√	
T5	GPIO0_B4	GPIO0_B4				I/O	I	up	4	√	
N5	GPIO0_B5/PMIC_SLEEP	GPIO0_B5	PMIC_SLEEP			I/O	I	down	4	√	
N1	GPIO0_B6/I2C3_SCL	GPIO0_B6	I2C3_SCL			I/O	I	up	4	√	

Pin	Pin Name	Func1	Func2	Func3	Func4	Pad Type①	Def①	Pull	Drive Strength②	INT②	DIE Power domain
M5	GPIO0_B7/TSADC_SHUT	GPIO0_B7	TSADC_SHUT			I/O	I	up	4	√	
M4	GPIO0_C0/PWM3/IR	GPIO0_C0	PWM3	IR		I/O	I	down	4	√	
U3	GPIO0_C1/HDMI_HPD1/CVBS_CLK_IN	GPIO0_C1	HDMI_HPD1	CVBS_CLK_IN		I/O	I	down	4	√	
U2	GPIO0_C2/I2C2_SDA/PMU_DEBUG1	GPIO0_C2	I2C4_SDA	PMU_DEBUG1		I/O	I	down	4	√	
P6	GPIO0_C3/PMU_DEBUG2	GPIO0_C3	PMU_DEBUG2			I/O	I	down	4	√	
T3	GPIO0_C4/PWM1/I2C3_SDA	GPIO0_C4	PWM1	I2C3_SDA		I/O	I	up	4	√	
T2	GPIO0_C5/PWM0/PMU_DEBUG3	GPIO0_C5	PWM0	PMU_DEBUG3		I/O	I	down	4	√	
R3	GPIO0_C6/PWM2/I2C2_SCL/PMU_DEBUG4	GPIO0_C6	PWM2	I2C4_SCL	PMU_DEBUG4	I/O	I	down	4	√	
Y9	GPIO1_A0/LCDC_D4/MIPI_CLKP	GPIO1_A0	LCDC_D4	MIPI_CLKP		A		NA		√	
W9	GPIO1_A1/LCDC_D5/MIPI_CLKN	GPIO1_A1	LCDC_D5	MIPI_CLKN		A		NA		√	
W11	GPIO1_A2/LCDC_D1/MIPI_D0P	GPIO1_A2	LCDC_D1	MIPI_D0P		A		NA		√	
Y11	GPIO1_A3/LCDC_D0/MIPI_D0N	GPIO1_A3	LCDC_D0	MIPI_D0N		A		NA		√	
W10	GPIO1_A4/LCDC_D3/MIPI_D1P	GPIO1_A4	LCDC_D3	MIPI_D1P		A		NA		√	
Y10	GPIO1_A5/LCDC_D2/MIPI_D1N	GPIO1_A5	LCDC_D2	MIPI_D1N		A		NA		√	
Y8	GPIO1_A6/LCDC_D6/MIPI_D2P	GPIO1_A6	LCDC_D6	MIPI_D2P		A		NA		√	MIPI_DSI
W8	GPIO1_A7/LCDC_D7/MIPI_D2N/PWM5	GPIO1_A7	LCDC_D7	MIPI_D2N	PWM5	A		NA		√	
Y7	GPIO1_B0/LCDC_D8/MIPI_D3P/PWM6	GPIO1_B0	LCDC_D8	MIPI_D3P	PWM6	A		NA		√	
W7	GPIO1_B1/LCDC_D9/MIPI_D3N/PWM7	GPIO1_B1	LCDC_D9	MIPI_D3N	PWM7	A		NA		√	
F17	GPIO1_B2/LCDC_D17/I2S_SDO/GMAC_TXD0	GPIO1_B2	LCDC_D17	I2S_SDO	GMAC_TXD0	I/O	I	down	8	√	
B20	GPIO1_B3/LCDC_D16/I2S_SCLK/GMAC_TXD1	GPIO1_B3	LCDC_D16	I2S_SCLK	GMAC_TXD1	I/O	I	down	8	√	
C19	GPIO1_B4/LCDC_D15/I2S_MCLK/GMAC_TXEN	GPIO1_B4	LCDC_D15	I2S_MCLK	GMAC_TXEN	I/O	I	down	8	√	
F18	GPIO1_B5/LCDC_D14/I2S_SDIO1/GMAC_RXD0	GPIO1_B5	LCDC_D14	I2S_SDIO1	GMAC_RXD0	I/O	I	down	8	√	
C20	GPIO1_B6/LCDC_D13/I2S_LRCLKTX/GMAC_RXD1	GPIO1_B6	LCDC_D13	I2S_LRCLKTX	GMAC_RXD1	I/O	I	down	8	√	APIO1 IO Voltage 3.3V/1.8V
G16	GPIO1_B7/LCDC_D12/I2S_SDIO2/GMAC_RXDV	GPIO1_B7	LCDC_D12	I2S_SDIO2	GMAC_RXDV	I/O	I	down	8	√	
E18	GPIO1_C0/LCDC_D11/I2S_LRCLKRX	GPIO1_C0	LCDC_D11	I2S_LRCLKRX		I/O	I	down	8	√	
E19	GPIO1_C1/LCDC_D10/I2S_SDI/PWM4	GPIO1_C1	LCDC_D10	I2S_SDI	PWM4	I/O	I	down	8	√	
D20	GPIO1_C2/LCDC_DEN/I2S_SDIO3/GMAC_RXER	GPIO1_C2	LCDC_DEN	I2S_SDIO3	GMAC_RXER	I/O	I	down	8	√	

Pin	Pin Name	Func1	Func2	Func3	Func4	Pad Type①	Def①	Pull	Drive Strength②	INT③	DIE Power domain
E20	GPIO1_C3/LCDC_VSYNC/GMAC_MDIO	GPIO1_C3	LCDC_VSYNC	GMAC_MDIO		I/O	I	down	8	√	
F19	GPIO1_C4/LCDC_HSYNC/GMAC_MDC	GPIO1_C4	LCDC_HSYNC	GMAC_MDC		I/O	I	down	8	√	
G17	GPIO1_C5/LCDC_CLK/GMAC_CLK	GPIO1_C5	LCDC_CLK	GMAC_CLK		I/O	I	down	8	√	
A18	GPIO1_D0/UART1_CTSN/SPI_CLK/DSP_TCK	GPIO1_D0	UART1_CTSN	SPI_CLK	DSP_TCK	I/O	I	down	4	√	
A19	GPIO1_D1/UART1_RTSN/SPI_CSN0/DSP_TMS	GPIO1_D1	UART1_RTSN	SPI_CSN0	DSP_TMS	I/O	I	up	4	√	
D19	GPIO1_D2/UART1_RX/SPI_RXD	GPIO1_D2	UART1_RX	SPI_RXD		I/O	I	up	4	√	
B18	GPIO1_D3/UART1_TX/SPI_TXD/DSP_TDO	GPIO1_D3	UART1_TX	SPI_TXD	DSP_TDO	I/O	I	down	4	√	
E17	5VGPIO1_D4/UART2_CTSN/HDMI_I2C0_SCL	5VGPIO1_D4	UART2_CTSN	HDMI_I2C0_SCL		I/O	I	up	4	√	
C17	5VGPIO1_D5/UART2_RTSN/HDMI_I2C0_SDA	5VGPIO1_D5	UART2_RTSN	HDMI_I2C0_SDA		I/O	I	up	4	√	
C18	5VGPIO1_D6/HDMI_HPD0	5VGPIO1_D6	HDMI_HPD0			I/O	I	down	4	√	
A20	GPIO1_D7/HDMI_CEC/DSP_RTCK	GPIO1_D7	HDMI_CEC	DSP_RTCK		I/O	I	up	4	√	
F16	GPIO2_D1/UART2_RX/JTAG_TMS	GPIO2_D1	UART2_RX	JTAG_TMS		I/O	I	up	4	√	
E16	GPIO2_D2/UART2_TX/JTAG_TCK	GPIO2_D2	UART2_TX	JTAG_TCK		I/O	I	up	4	√	
T19	GPIO2_D3/I2C1_SDA	GPIO2_D3	I2C1_SDA			I/O	I	up	4	√	
R17	GPIO2_D4/I2C1_SCL	GPIO2_D4	I2C1_SCL			I/O	I	up	4	√	
M19	GPIO2_D5/SDIO_CLKO	GPIO2_D5	SDIO_CLKO			I/O	I	down	4	√	
L20	GPIO2_D6/SDIO_CMD	GPIO2_D6	SDIO_CMD			I/O	I	up	8	√	
L19	GPIO2_D7/SDIO_D0	GPIO2_D7	SDIO_D0			I/O	I	up	8	√	
M18	GPIO3_A0/SDIO_D1	GPIO3_A0	SDIO_D1			I/O	I	up	8	√	
M20	GPIO3_A1/SDIO_D2	GPIO3_A1	SDIO_D2			I/O	I	up	8	√	
M17	GPIO3_A2/SDIO_D3	GPIO3_A2	SDIO_D3			I/O	I	up	8	√	
R20	GPIO3_A3/UART0_RTSN	GPIO3_A3	UART0_RTSN			I/O	I	up	4	√	
P18	GPIO3_A4/UART0_CTSN	GPIO3_A4	UART0_CTSN			I/O	I	up	4	√	
T20	GPIO3_A5/UART0_RX	GPIO3_A5	UART0_RX			I/O	I	up	4	√	APIO2 IO Vlotage 3.3V/1.8V
P17	GPIO3_A6/UART0_TX	GPIO3_A6	UART0_TX			I/O	I	up	4	√	
P19	GPIO3_A7	GPIO3_A7				I/O	I	down	4	√	
U20	GPIO3_B0	GPIO3_B0				I/O	I	down	4	√	
N16	GPIO3_B1/PCM_OUT/FLASH_TRIG_OUT	GPIO3_B1	PCM_OUT	FLASH_TRIG_OUT		I/O	I	down	4	√	
N18	GPIO3_B2/PCM_IN/FLASH_TRIG_IN	GPIO3_B2	PCM_IN	FLASH_TRIG_IN		I/O	I	down	4	√	
R19	GPIO3_B3/PCM_CLK	GPIO3_B3	PCM_CLK			I/O	I	down	4	√	
N20	GPIO3_B4/PCM_SYNC/PRELIGHT_TRIG_OUT	GPIO3_B4	PCM_SYNC	PRELIGHT_TRIG_OUT		I/O	I	down	4	√	
P20	GPIO3_B5/MIPI_CSI_MCLK	GPIO3_B5	MIPI_CSI_MCLK			I/O	I	down	4	√	

Pin	Pin Name	Func1	Func2	Func3	Func4	Pad Type①	Def①	Pull	Drive Strength②	INT③	DIE Power domain
N19	GPIO3_B6	GPIO3_B6				I/O	I	down	4	√	
D11	GPIO3_B7/SDMMC0_PWR	GPIO3_B7	SDMMC0_PWR			I/O	I	down	8	√	APIO3 IO Voltage 3.3V/1.8V
C12	GPIO3_C0/SDMMC0_D3	GPIO3_C0	SDMMC0_D3			I/O	I	up	8	√	
D12	GPIO3_C1/SDMMC0_D2	GPIO3_C1	SDMMC0_D2	UART2_RX		I/O	I	up	8	√	
A12	GPIO3_C2/SDMMC0_D1/UART2_RX	GPIO3_C2	SDMMC0_D1	UART2_TX		I/O	I	up	8	√	
B12	GPIO3_C3/SDMMC0_D0/UART2_TX	GPIO3_C3	SDMMC0_D0			I/O	I	up	8	√	
B13	GPIO3_C4/SDMMC0_CLKO	GPIO3_C4	SDMMC0_CLKO			I/O	I	up	8	√	
A13	GPIO3_C5/SDMMC0_CMD	GPIO3_C5	SDMMC0_CMD			I/O	I	down	4	√	
V20	GPIO1_C6/CIF_D4/I2S_LRCLKTX	GPIO1_C6	CIF_D4	I2S_LRCLKTX		I/O	I	down	8	√	APIO5 IO Voltage 3.3V/1.8V
U19	GPIO1_C7/CIF_D5/I2S_SDIO2	GPIO1_C7	CIF_D5	I2S_SDIO2		I/O	I	down	8	√	
Y19	GPIO2_C0/CIF_D6/I2S_LRCLKRX	GPIO2_C0	CIF_D6	I2S_LRCLKRX		I/O	I	down	8	√	
U14	GPIO2_C1/CIF_D7/I2S_SDI	GPIO2_C1	CIF_D7	I2S_SDI		I/O	I	down	8	√	
V16	GPIO2_C3/CIF_D0/I2S_SDO	GPIO2_C3	CIF_D0	I2S_SDO		I/O	I	down	8	√	
U16	GPIO2_C4/CIF_D1/I2S_SCLK	GPIO2_C4	CIF_D1	I2S_SCLK		I/O	I	down	8	√	
U15	GPIO2_C5/CIF_D2/I2S_MCLK	GPIO2_C5	CIF_D2	I2S_MCLK		I/O	I	down	8	√	
V14	GPIO2_C6/CIF_D3/I2S_SDIO1	GPIO2_C6	CIF_D3	I2S_SDIO1		I/O	I	down	8	√	
V19	GPIO3_C6/CIF_VSYNC	GPIO3_C6	CIF_VSYNC			I/O	I	down	8	√	
T18	GPIO3_C7/CIF_CLKIN	GPIO3_C7	CIF_CLKIN			I/O	I	down	8	√	
U18	GPIO3_D0/CIF_HREF	GPIO3_D0	CIF_HREF			I/O	I	down	8	√	
T17	GPIO3_D1/CIF_PDN	GPIO3_D1	TCIF_PDN			I/O	I	down	8	√	
V18	GPIO3_D2/CIF_CLKOUT	GPIO3_D2	CIF_CLKOUT			I/O	I	down	8	√	
Y20	GPIO3_D3/CIF_D8/I2S_SDIO3	GPIO3_D3	CIF_D8	I2S_SDIO3		I/O	I	down	8	√	
U17	GPIO3_D4/CIF_D9/FLASH_TRIG_IN	GPIO3_D4	CIF_D9	FLASH_TRIG_IN		I/O	I	down	8	√	
R16	GPIO3_D5/CIF_D10/FLASH_TRIG_OUT	GPIO3_D5	CIF_D10	FLASH_TRIG_OUT		I/O	I	down	8	√	
W20	GPIO3_D6/CIF_D11/PRELIGHT_TRIG_OUT	GPIO3_D6	CIF_D11	PRELIGHT_TRIG_OUT		I/O	I	down	8	√	
K18	GPIO2_A0/FLASH_D0/EMMC_D0/SFC_SIO_IO0	GPIO2_A0	FLASH_D0	EMMC_D0	SFC_SIO_IO0	I/O	I	up	8	√	APIO6 IO Voltage 3.3V/1.8V
J16	GPIO2_A1/FLASH_D1/EMMC_D1/SFC_SIO_IO1	GPIO2_A1	FLASH_D1	EMMC_D1	SFC_SIO_IO1	I/O	I	up	8	√	
K17	GPIO2_A2/FLASH_D2/EMMC_D2/SFC_WP_IO2	GPIO2_A2	FLASH_D2	EMMC_D2	SFC_WP_IO2	I/O	I	up	8	√	
H19	GPIO2_A3/FLASH_D3/EMMC_D3/SFC_HOLD_IO3	GPIO2_A3	FLASH_D3	EMMC_D3	SFC_HOLD_IO3	I/O	I	up	8	√	
G20	GPIO2_A4/FLASH_D4/EMMC_D4	GPIO2_A4	FLASH_D4	EMMC_D4		I/O	I	up	8	√	
J19	GPIO2_A5/FLASH_D5/EMMC_D5	GPIO2_A5	FLASH_D5	EMMC_D5		I/O	I	up	8	√	

Pin	Pin Name	Func1	Func2	Func3	Func4	Pad Type①	Def①	Pull	Drive Strength①	INT①	DIE Power domain
L16	GPIO2_A6/FLASH_D6/EMMC_D6	GPIO2_A6	FLASH_D6	EMMC_D6		I/O	I	up	8	√	
H20	GPIO2_A7/FLASH_D7/EMMC_D7	GPIO2_A7	FLASH_D7	EMMC_D7		I/O	I	up	8	√	
H18	GPIO2_B0/FLASH_ALE	GPIO2_B0	FLASH_ALE			I/O	I	down	8	√	
F20	GPIO2_B1/FLASH_CLE	GPIO2_B1	FLASH_CLE			I/O	I	down	8	√	
K19	GPIO2_B2/FLASH_WRN	GPIO2_B2	FLASH_WRN			I/O	I	up	8	√	
L17	GPIO2_B3/FLASH_RDN	GPIO2_B3	FLASH_RDN			I/O	I	up	8	√	
G19	GPIO2_B4/FLASH_RDY/EMMC_CMD/SFC_CSN0	GPIO2_B4	FLASH_RDY	EMMC_CMD	SFC_CSN0	I/O	I	up	8	√	
J20	GPIO2_B5/FLASH_CSN0	GPIO2_B5	FLASH_CSN0			I/O	I	up	8	√	
K20	GPIO2_B6/EMMC_CLKO	GPIO2_B6	EMMC_CLKO			I/O	I	down	8	√	
J18	GPIO2_B7/FLASH_CSN1/SFC_CLK	GPIO2_B7	FLASH_CSN1	SFC_CLK		I/O	I	up	8	√	
H17	GPIO2_C2/FLASH_WP/EMMC_PWR	GPIO2_C2	FLASH_WP	EMMC_PWR		I/O	I	down	8	√	
W14	MIPI_CSI_D0N	MIPI_CSI_D0N				A		NA			MIPI_CSI
Y14	MIPI_CSI_D0P	MIPI_CSI_D0P				A		NA			
W15	MIPI_CSI_D1N	MIPI_CSI_D1N				A		NA			
Y15	MIPI_CSI_D1P	MIPI_CSI_D1P				A		NA			
W17	MIPI_CSI_D2N	MIPI_CSI_D2N				A		NA			
Y17	MIPI_CSI_D2P	MIPI_CSI_D2P				A		NA			
Y18	MIPI_CSI_D3N	MIPI_CSI_D3N				A		NA			
W18	MIPI_CSI_D3P	MIPI_CSI_D3P				A		NA			
W16	MIPI_CSI_CLKP	MIPI_CSI_CLKP				A		NA			
Y16	MIPI_CSI_CLKN	MIPI_CSI_CLKN				A		NA			
U12	MIPI_CSI_EXTR	MIPI_CSI_EXTR				A		NA			
P7	TEST	TEST				I		down			PMUIO 3.3V
T1	NPOR	NPOR				I		up			
P2	XOUT_24M	XOUT_24M				O		NA			PLL_1V0
P1	XIN_24M	XIN_24M				I		NA			
Y1	HDMI_TXCN	HDMI_TXCN				A		NA			HDMI
W1	HDMI_TXCP	HDMI_TXCP				A		NA			
W2	HDMI_TX0N	HDMI_TX0N				A		NA			
W3	HDMI_TX0P	HDMI_TX0P				A		NA			
W4	HDMI_TX1N	HDMI_TX1N				A		NA			
Y4	HDMI_TX1P	HDMI_TX1P				A		NA			
Y5	HDMI_TX2N	HDMI_TX2N				A		NA			
W5	HDMI_TX2P	HDMI_TX2P				A		NA			
U6	HDMI_EXTR	HDMI_EXTR				A		NA			
W13	USB1_DP	USB1_DP				A		NA			USB
Y13	USB1_DM	USB1_DM				A		NA			
U10	USB_EXTR	USB_EXTR				A		NA			
V12	USB_VBUS	USB_VBUS				A		NA			
V11	USB0_ID	USB0_ID				A		NA			
Y12	USB0_DM	USB0_DM				A		NA			

Pin	Pin Name	Func1	Func2	Func3	Func4	Pad Type①	Def③	Pull	Drive Strength②	INT④	DIE Power domain
W12	USB0_DP	USB0_DP				A		NA			
A17	CODEC_MICBIAS	CODEC_MICBIAS				A		NA			Audio Codec
C15	CODEC_MICL	CODEC_MICL				A		NA			
B15	CODEC_MICR	CODEC_MICR				A		NA			
B16	CODEC_VCM	CODEC_VCM				A		NA			
A15	CODEC_AOL	CODEC_AOL				A		NA			
A16	CODEC_AOR	CODEC_AOR				A		NA			
A14	VIDEO_IN_P	VIDEO_IN_P				A		NA			VADC_AVDD
B14	VIDEO_IN_N	VIDEO_IN_N				A		NA			
W6	VDAC_EXTR	VDAC_EXTR				P		NA			VDAC_AVDD
Y6	VDAC_OUT	VDAC_OUT				A		NA			
D13	ADC_IN0	ADC_IN0				A		NA			SAR_AVDD_18
E13	ADC_IN1	ADC_IN1				A		NA			
E12	ADC_IN2	ADC_IN2				A		NA			
D10	ADC_IN3	ADC_IN3				A		NA			
F12	ADC_IN4	ADC_IN4				A		NA			
E11	ADC_IN5	ADC_IN5				A		NA			
N3	EFUSE	EFUSE				P		NA			EFUSE
E4	PZQ	PZQ				A		NA			
F6	VREF	VREF				A		NA			
J6	DDR_VDD_1	DDR_VDD_1				A		NA			
H6	DDR_VDD_2	DDR_VDD_2				A		NA			
G6	DDR_VDD_3	DDR_VDD_3				A		NA			
E10	DDR_VDD_4	DDR_VDD_4				A		NA			
F7	DDR_VDD_5	DDR_VDD_5				A		NA			
F8	DDR_VDD_6	DDR_VDD_6				A		NA			
F9	DDR_VDD_7	DDR_VDD_7				A		NA			

Notes:

①:Type: I = input, O = output, I/O = input/output (bidirectional)
AP = Analog Power, AG = Analog Ground
DP = Digital Power, DG = Digital Ground
A = Analog
②:Output Drive Unit is mA, only Digital IO has drive value;
③:Def: I = input without any pull resistor, O = output without any pull resistor;
④:INT: interrupt

2.8 IO Pin Name Description

This sub-chapter will focus on the detailed function description of every pins based on different interface.

2.8.1 MISC

Interface	Pin Name	Direction	Description
Misc	XIN_24M	I	Clock input of 24MHz crystal

Interface	Pin Name	Direction	Description
	XOUT_24M	O	Clock output of 24MHz crystal
	NPOR	I	Chip hardware reset

2.8.2 JTAG

Interface	Pin Name	Direction	Description
SWJ-DP	JTAG_TMS	I/O	JTAG interface TMS input/SWD interface data out
	JTAG_TCK	I	JTAG interface clock input/SWD interface clock input

2.8.3 SDMMC

Interface	Pin Name	Direction	Description
SDMMC Host Controller	SDMMC0_D*i*(*i*=0~3)	I/O	sdmmc card data input and output
	SDMMC0_CLKO	O	sdmmc card clock
	SDMMC0_CMD	I/O	sdmmc card command output and response input
	SDMMC0_DET	I	sdmmc card detect signal, 0 represents presence of card

2.8.4 SDIO

Interface	Pin Name	Direction	Description
SDIO Host Controller	SDIO_CLKO	O	sdio clock
	SDIO_CMD	I/O	sdio command output and response input
	SDIO_DATA*i*(*i*=0~3)	I/O	sdio data input and output

2.8.5 EMMC

Interface	Pin Name	Direction	Description
EMMC Interface	EMMC_CLKO	O	emmc card clock
	EMMC_CMD	I/O	emmc card command output and response input
	EMMC_DATA*i*(*i*=0~7)	I/O	emmc card data input and output

2.8.6 DDR3

Following table is for RV1108A.

Interface	Pin Name	Direction	Description
DMC	DDR_CLK	O	Active-high clock signal to the memory device.
	DDR_CLKn	O	Active-low clock signal to the memory device.
	DDR_CKE	O	Active-high clock enable signal to the memory device
	DDR_CSN	O	Active-low chip select signal to the memory device. There are two chip select.
	DDR_RASN	O	Active-low row address strobe to the memory device.
	DDR_CASN	O	Active-low column address strobe to the memory device.
	DDR_WEN	O	Active-low write enable strobe to the memory device.
	DDR_RESET	O	DDR3 reset signal to the memory device
	DDR_Ba*i*(*i*=0,1,2)	O	Bank address signal to the memory device.
	DDR_A*i*(*i*=0~14)	O	Address signal to the memory device.
	DDR_ODT0	O	On-Die Termination output signal for two chip select.

Interface	Pin Name	Direction	Description
	DDR_Dm*i*(*i*=0,1)	O	Active-low data mask signal to the memory device.
	DDR_DQS0/1	I/O	Active-high bidirectional data strobes to the memory device.
	DDR_DQS0n/1n	I/O	Active-low bidirectional data strobes to the memory device.
	DDR_Dq*i*(*i*=0~15)	I/O	Bidirectional data line to the memory device.

2.8.7 NAND FLASH

Interface	Pin Name	Direction	Description
NAND	FLASH_ALE	O	Flash address latch enable signal
	FLASH_CLE	O	Flash command latch enable signal
	FLASH_WRN	O	Flash write enable and clock signal
	FLASH_RDN	O	Flash read enable and write/read signal
	FLASH_RDY	I	Flash ready/busy signal
	FLASH_Cs*i*(*i*=0,1)	O	Flash chip enable signal for chip
	FLASH_WP	O	Flash write-protected signal
	FLASH_DATA*i*(*i*=0~7)	I/O	Flash data inputs/outputs signal

2.8.8 SPI FLASH

Interface	Pin Name	Direction	Description
SPI Flash	SFC_SIO_IO0	I/O	Data Input Output 0
	SFC_SIO_IO1	I/O	Data Input Output 1
	SFC_WP_IO2	I/O	Write Protect Output (Data Input Output 2)
	SFC_HOLD_IO3	I/O	Hold t Input (Data Input Output 3)
	SFC_CSN0	O	Chip Select
	SFC_CLK	O	Serial Clock Output

2.8.9 PCM

Interface	Pin Name	Direction	Description
PCM	PCM_OUT	O	PCM serial data output
	PCM_IN	I	PCM serial data input
	PCM_CLK	O	PCM clock source
	PCM_SYNC	I/O	PCM serial data synchronous

2.8.10 I2S

Interface	Pin Name	Direction	Description
I2S Controller	I2S_SCLK	I/O	I2S serial clock
	I2S_MCLK	O	I2S clock source
	I2S_LRCLKTX	I/O	I2S left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode
	I2S_SDIOi(i=0~3)	O	I2S serial data output
	I2S_LRCLKRX	I/O	I2S left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode
	I2S_SDI	I/O	I2S serial data input

2.8.11 SPI

Interface	Pin Name	Direction	Description
SPI Controller	SPI_CLK	I/O	SPI serial clock
	SPI_CSN0	I/O	SPI chip select signal ,low active
	SPI_TXD	O	SPI serial data output
	SPI_RXD	I	SPI serial data input

2.8.12 PWM

Interface	Pin Name	Direction	Description
PWM	PWM0	O	Pulse Width Modulation output
	PWM1	O	Pulse Width Modulation output
	PWM2	O	Pulse Width Modulation output
	PWM3	O	Pulse Width Modulation output
	PWM4	O	Pulse Width Modulation output
	PWM5	O	Pulse Width Modulation output
	PWM6	O	Pulse Width Modulation output
	PWM7	O	Pulse Width Modulation output

2.8.13 I2C

Interface	Pin Name	Direction	Description
I2C	I2C0_SDA	I/O	I2C0 data
	I2C0_SCL	I/O	I2C0 clock
	I2C1_SDA	I/O	I2C1 data
	I2C1_SCL	I/O	I2C1 clock
	I2C2_SDA	I/O	I2C2 data
	I2C2_SCL	I/O	I2C2 clock
	I2C3_SDA	I/O	I2C3_data
	I2C3_SCL	I/O	I2C3 clock

2.8.14 UART

Interface	Pin Name	Direction	Description
UART	UART1_CTSN	I	UART1 clear to send
	UART1_RTSN	O	UART1 request to send
	UART1_RX	I	UART1 serial data input
	UART1_TX	O	UART1 serial data output
	UART2_CTSN	I	UART2 clear to send
	UART2_RTSN	O	UART2 request to send
	UART2_RX	I	UART2 serial data input
	UART2_TX	O	UART2 serial data output
	UART0_CTSN	I	UART0 clear to send
	UART0_RTSN	O	UART0 request to send
	UART0_RTX	I	UART0 serial data input
	UART0_TX	O	UART0 serial data output

2.8.15 GMAC

Interface	Pin Name	Direction	Description
GMAC	GMAC_TXD*i*(*i*=0~1)	O	GMAC TX data
	GMAC_RXD*i*(*i*=0~1)	I	GMAC RX data

	GMAC_TXEN	O	GMAC TX data enable
	GMAC_RXDV	I	Collision and Data Valid
	GMAC_RXER	I	GMAC RX error signal
	GMAC_MDIO	I/O	GMAC management interface data
	GMAC_MDC	O	GMAC management interface clock
	GMAC_CLK	I/O	RMII REC_CLK output or GMAC external clock input

2.8.16 USB

Interface	Pin Name	Direction	Description
USB OTG 2.0	USB0_DM	I/O	USB OTG 2.0 Data signal DM
	USB0_DP	I/O	USB OTG 2.0 Data signal DP

Interface	Pin Name	Direction	Description
USB HOST 2.0	USB1_DP	I/O	USB HOST 2.0 Data signal DP
	USB1_DM	I/O	USB HOST 2.0 Data signal DM

2.8.17 EFUSE

Interface	Pin Name	Direction	Description
EFUSE	EFUSE	N/A	eFuse program and sense power

2.8.18 HDMI

Interface	Pin Name	Direction	Description
HDMI	HDMI_TX0N	O	TMDS channel 0 negative data line
	HDMI_TX0P	O	TMDS channel 0 positive data line
	HDMI_TX1N	O	TMDS channel 1 negative data line
	HDMI_TX1P	O	TMDS channel 1 positive data line
	HDMI_TX2N	O	TMDS channel 2 negative data line
	HDMI_TX2P	O	TMDS channel 2 positive data line
	HDMI_EXTR	O	Connect 2.0Kohm resistor to ground to generate reference current
	HDMI_HPD0	I/O	HDMI hot plug detect signal
	HDMI_CEC	I/O	HDMI CEC signal

2.8.19 CODEC

Interface	Pin Name	Direction	Description
CODEC	CODEC_MICL	I	Left channel input
	CODEC_MICR	I	Right channel input
	CODEC_VCM	I	Reference voltage input
	CODEC_AOL	O	Left channel output
	CODEC_AOR	O	Right channel output

2.8.20 CVBSIN

Interface	Pin Name	Direction	Description
CVBSIN	VIDEO_IN_P	I	Data signal P
	VIDEO_IN_N	I	Data signal N

2.8.21 CVBSOUT

Interface	Pin Name	Direction	Description
CVBSOUT	VDAC_EXTR	I	Connect external resistor to generate current reference
	VDAC_OUT	O	Data signal output

2.8.22 SAR-ADC

Interface	Pin Name	Direction	Description
SAR-ADC	ADC_In*i*(*i*=0~5)	I	Analog input

2.8.23 ADC

Interface	Pin Name	Direction	Description
ADC	ADC_In*i*(*i*=0~5)	I	Analog input

2.8.24 CIF

Interface	Pin Name	Direction	Description
Camera IF	CIF_D*i*(*i*=0~11)	I	Camera interface input pixel data
	CIF_VSYNC	I	Camera interface vertical sync signal
	CIF_CLKIN	I	Camera interface input pixel clock
	CIF_HREF	I	Camera interface horizontal sync signal
	CIF_PDN	O	Camera power down control output
	CIF_CLKOUT	O	Camera interface output work clock

2.8.25 MIPI

Interface	Pin Name	Direction	Description
MIPI_DSI	MIPI_CLKP	I/O	MIPI DSI positive differential clock line transceiver output
	MIPI_CLKN	I/O	MIPI DSI negative differential clock line transceiver output
	MIPI_D*i*P(*i*=0~3)	I/O	MIPI DSI positive differential data line transceiver output
	MIPI_D*i*N(i=0~3)	I/O	MIPI DSI negative differential data line transceiver output

Interface	Pin Name	Direction	Description
MIPI_CSI	MIPI_CSI_D*i*N(i=0~3)	I/O	MIPI CSI negative differential data line transceiver output
	MIPI_CSI_D*i*P(i=0~3)	I/O	MIPI CSI positive differential data line transceiver output
	MIPI_CSI_CLKP	I/O	MIPI CSI positive differential clock line transceiver output
	MIPI_CSI_CLKN	I/O	MIPI CSI negative differential clock line transceiver output
	MIPI_CSI_EXTR	I/O	MIPI CSI external resistor connection. Recommend to use a 2 KΩ E96 resistor.

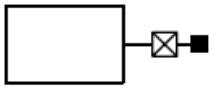
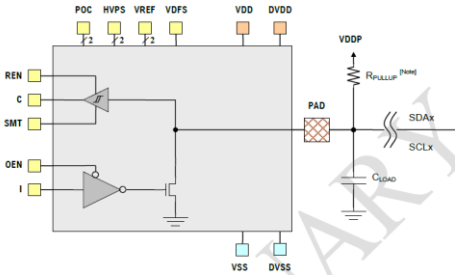
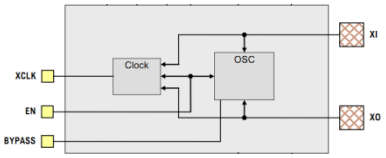
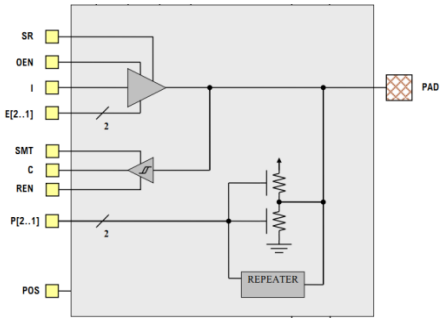
2.8.26 LCDC

Interface	Pin Name	Direction	Description
LCDC	LCDC_Di(i=0~17)	O	LCDC data line transceiver output
	LCDC_DEN	I/O	LCDC data enable
	LCDC_VSYNC	I/O	LCDC vertical sync signal output
	LCDC_HSYNC	I/O	LCDC horizontal sync signal output
	LCDC_CLK	I/O	LCDC pixel clk output

2.9 RV1108 IO Type

The following list shows IO type except DDR IO and all of Power/Ground IO.

Table 2-7 RV1108 IO Type List

Type	Diagram	Description	Pin Name
A		Analog IO Cell with IO voltage	EFUSE_VQPS
B		Pad for 5V tolerance	hdmi_ddcscl hdmi_ddcsda hdmi_hpd
C		Crystal Oscillator with high enable	XIN24M/XOUT24M
D		Tri-state output pad with input, which pull-up/pull-down, slew rate and drive strength is configurable	Pad of digital GPIO

Chapter 3 Electrical Specification

3.1 Absolute Maximum Ratings

Table 3-1 RV1108 absolute maximum ratings

Parameters	Related Power Group	Max	Unit
DC supply voltage for Digital GPIO	APIO1_VDD APIO2_VDD APIO3_VDD PMUIO_VDD APIO5_VDD APIO6_VDD	3.6	V
DC supply voltage for DDR IO	DDR_VDD	1.65	V
DC supply voltage for digital part of PLL	PLL_AVDD_1V0	1.1	V
DC supply voltage for Analog part of PLL	PLL_AVDD_1V8	1.98	V
DC supply voltage for Analog part of USB OTG/Host2.0	USB_AVDD_1V0 USB_AVDD_1V8 USB_AVDD_3V3	1.1 1.98 3.63	V
DC supply voltage for Analog part of Audio Codec	CODEC_AVDD_1V8	1.98	V
DC supply voltage for Analog part of VDAC	VDAC_AVDD_1V8	1.98	V
DC supply voltage for Analog part of HDMI	HDMI_AVDD_1V0 HDMI_AVDD_1V8	1.1 1.98	V
DC supply voltage for Analog part of SARADC and TSADC	SADC_AVDD_1V8	1.98	V
DC supply voltage for Analog part of DSI	MIPI_DSI_AVDD_1V0 MIPI_DSI_AVDD_1V8 MIPI_DSI_AVDD_3V3	1.1 1.8	V
DC supply voltage for Analog part of CSI	MIPI_CSI_AVDD_1V0	1.1	V
DC supply voltage for Digital part of VIDEOADC	VIDEO_AVDD_1V0	1.1	V
DC supply voltage for Analog part of VIDEOADC	VIDEO_AVDD_1V8	1.98	V
DC supply voltage for Analog part of EFUSE	EFUSE	1.65	V
Analog Input voltage for DP/DM/VBUS of USB OTG/Host2.0		5	V
Digital input voltage for input buffer of GPIO		3.6	V
Digital output voltage for output buffer of GPIsO		3.6	V
Highest Storage Temperature	Tstg	125	℃
Lowest Storage Temperature	Tstg	-40	℃
Max Conjunction Temperature	Tj	125	℃

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

3.2 Recommended Operating Condition

Following table describes the recommended operating condition.

Table 3-2 RV1108 recommended operating condition

Parameters	Symbol①	Min	Typ	Max	Units
Internal digital logic Power	CORE_VDD PMU_VDD	0.9	1.0	1.1	V

Parameters	Symbol①	Min	Typ	Max	Units
Max frequency of Cortex A7 CPU	Frequency			1.0	GHz
Max frequency of DSP	Frequency			600	MHz
Digital GPIO Power(3.3V/2.5V/1.8V)	APIO1_VDD APIO2_VDD APIO3_VDD PMUIO_VDD APIO5_VDD APIO6_VDD	3 2.25 1.62	3.3 2.5 1.8	3.6 2.75 1.98	V
DDR IO (DDR3 mode) Power	DDR_VDD	1.425	1.5	1.575	V
DDR IO (DDR3L mode) Power	DDR_VDD	1.283	1.35	1.417	V
PLL Digital Power	PLL_AVDD_1V0	0.9	1.0	1.1	V
PLL Analog Power	PLL_AVDD_1V8	1.62	1.8	1.98	V
ACODEC Analog Power	CODEC_AVDD_1V8	1.62	1.8	1.98	V
VDAC Analog Power	VDAC_AVDD_1V8	1.62	1.8	1.98	V
USB OTG/Host2.0 Digital Power	USB_AVDD_1V0	0.9	1.0	1.1	V
USB OTG/Host2.0 Analog Power(1.8V)	USB_AVDD_1V8	1.62	1.8	1.98	V
USB OTG/Host2.0 Analog Power(3.3V)	USB_AVDD_3V3	3.069	3.3	3.63	V
HDMI Analog Power(1.0V)	HDMI_AVDD_1V0	0.9	1.0	1.1	V
HDMI Analog Power(1.8V)	HDMI_AVDD_1V8	1.62	1.8	1.98	V
SARADC Analog Power(1.8V)	SADC_AVDD_1V8	1.62	1.8	1.98	V
TSADC Analog Power(1.8V)	SADC_AVDD_1V8	1.62	1.8	1.98	V
MIPI DSI Analog Power(1.0V)	MIPI_DSI_AVDD_1V0	0.9	1.0	1.1	V
MIPI DSI Analog Power(1.8V)	MIPI_DSI_AVDD_1V8	1.62	1.8	1.98	V
MIPI DSI Analog Power(3.3V)	MIPI_DSI_AVDD_3V3	3.069	3.3	3.63	V
MIPI CSI Analog Power(1.0V)	MIPI_CSI_AVDD_1V0	0.9	1.0	1.1	V
VIDEOADC Analog Power(1.0V)	VIDEO_AVDD_1V0	0.9	1.0	1.1	V
VIDEOADC Analog Power(1.8V)	VIDEO_AVDD_1V8	1.62	1.8	1.98	V
PLL input clock frequency		N/A	24	N/A	MHz
Ambient Operating Temperature for RV1108A & RV1108G		0	25	80	℃
Ambient Operating Temperature for RV1108K1		-40	25	85	℃

Notes:① Symbol name is same as the pin name in the io descriptions

3.3 DC Characteristics

Table 3-3 RV1108 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Units
Digital GPIO @3.3V	Input Low Voltage	Vil	-0.3	0	3.3x0.3	V
	Input High Voltage	Vih	3.3x0.7	3.3	3.3+0.3	V
	Output Low Voltage	Vol	-0.3	NA	NA	V

Parameters		Symbol	Min	Typ	Max	Units
	Output High Voltage	Voh	NA	NA	3.6	V
	Pullup Resistor	Rpu	33.7	58	101.5	Kohm
	Pulldown Resistor	Rpd	34.2	60.1	109.3	Kohm
Digital GPIO @1.8V	Input Low Voltage	Vil	-0.3	0	1.8x0.3	V
	Input High Voltage	Vih	1.8x0.7	1.8	1.8 + 0.3	V
	Output Low Voltage	Vol	-0.3	NA	NA	V
	Output High Voltage	Voh	NA	NA	1.8+0.3	V
	Pullup Resistor	Rpu	35	62.9	120	Kohm
	Pulldown Resistor	Rpd	35.1	61	113.9	Kohm
DDR IO @DDR3 mode	Input High Voltage	Vih_ddr	VREF + 0.10	NA	DDR_VDD+0.4	V
	Input Low Voltage	Vil_ddr	-0.4	NA	VREF - 0.10	V
	Output High Voltage	Voh_ddr	0.9xDDR_VDD	NA	N/A	V
	Output Low Voltage	Vol_ddr	N/A	NA	0.1*DDR_VDD	V
	Input termination resistance(ODT) to VDDIO_DDRi/2 (i=0~6)	Rtt	100 54 36	120 60 40	140 66 44	Ohm
HDMI	Single-ended standby voltage	Voff	avddtmds±10			mV
	Single-ended output swing voltage RT=50Ω	Vswing	400		600	mV
		Vswing_data	400		600	mV
		Vswing_clock	400		600	mV
	Single-ended output high voltage	Vh				mV
			avddtmds-400		avddtmds+10	mV
		Vh_data	avddtmds-400		avddtmds+10	mV
		Vh_clock	avddtmds-400		avddtmds+10	mV
	Single-ended output low voltage	Vl				mV
			avddtmds-1000		avddtmds-400	mV
		Vl_data	avddtmds-1000		avddtmds-400	mV
		Vl_clock	avddtmds-1000		avddtmds-400	mV
	Differential source termination load	Rterm	75		150	Ω
MIPI DSI MIPI mode	HS TX static common-mode	Vcmtx	150	200	250	mV
	Vcmtx mismatch when output is Differential-1 or Differential-0	ΔVcmtx(1,0)			5	mV

Parameters		Symbol	Min	Typ	Max	Units
	HS Transmit differential voltage	Vod	140	200	270	mV
	Vod mismatch when output is Differential-1 or Differential-0	ΔVod			10	mV
	HS output high voltage	Vohhs			360	mV
	Single ended output impedance	Zos	40	50	62.5	Ohm
	Single ended output impedance mismacth	ΔZos			10	%
MIPI DSI LP mode	The venin output high level	Voh	0.9	1	1.1	V
	The venin output low level	Vol	-50		50	mV
	Output impedance of LP	Zolp	110			Ω
MIPI DSI CMOS mode	High-level output voltage	Voh	3	3.3		V
	Low-level output voltage	Vol		0	0.2	V
	Output impedance	Zolp	40		460	Ω
MIPI CSI MIPI mode	Common-mode voltage HS receive mode	Vcmrx(dc)	70		300	mV
	Differential input high threshold	Vidth			70	mV
	Differential input low threshold	Vidtl	-70			mV
	Single-ended input high voltage	Vihhs			460	mV
	Single-ended input low voltage	Vilhs	-40			mV
	Single-ended threshold for HS termination enable	Vterm-en			450	mV
	Differential input impedance	Zid	80	100	125	Ω
MIPI CSI LP mode	Logic 1 input voltage	Vih	880			mV
	Logic 0 input voltage, not in ULP state	Vil			550	mV
	Logic 0 input voltage, ULP state	Vil-ulps			300	mV
	Input hysteresis	Vhyst	25			mV
SARADC	Effective Number of Bit	ENOB		9		Bit
	Differential Nonlinearity	DNL	-1		+1	LSB
	Integral Nonlinearity	INL	-2		+2	LSB
	Input Voltage Range	Vin	0		1	AVDD
	Input Capacitance	Cin		10		pF
	Sampling rate	fs			1	MS/s
	Spurious Free Dynamic Range	SFDR		61		dB
	Signal to Noise and Harmonic Ratio	SNDR		56		dB
CODEC	Microphone Bias	Vmicb	0.5 * AVDD		0.85 * AVDD	V
		Imicb			3	mA
	Microphone Gain Boost PGA	Gbst	0		20	dB
		Cin		10		pF
	ALC PGA	Galc	-18		28.5	dB
	ADC	SNR		92		dB
		THD		-81		dB
	DAC Output Driver	Gdrv	-39		6	dB
		Rout		1		Ω
		Cout		20		pF

Parameters		Symbol	Min	Typ	Max	Units
		PSRR		70		

3.4 Electrical Characteristics for General IO

Table 3-4 RV1108 Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Units
Digital GPIO @3.3V	Input leakage current	Ii	Vin = 3.3V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 3.3V, pulldown disabled	NA	NA	10	uA
			Vin = 3.3V, pulldown enabled	NA	NA	106.4	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	10	uA
			Vin = 0V, pullup enabled	NA	NA	107.8	uA
Digital GPIO @1.8V	Input leakage current	Ii	Vin = 1.8V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 1.8V, pulldown disabled	NA	NA	10	uA
			Vin = 1.8V, pulldown enabled	NA	NA	61.3	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	10	uA
			Vin = 0V, pullup enabled	NA	NA	61.4	uA

3.5 Electrical Characteristics for PLL

Table 3-5 RV1108 Electrical Characteristics for PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Units
PLL	Input clock frequency(Int)	F_{in}	Fin = FREF @3.3V/1.1V	1		800	MHz
	Input clock frequency(Frac)	F_{in}	Fin = FREF @3.3V/1.1V	10		800	MHz
	VCO operating range	F_{vco}	Fvco = Fref * FBDIV @3.3V/1.1V	800		3200	MHz
	Output clock frequency	F_{out}	Fout = Fvco/POSTDIV @3.3V/1.1V	16		3200	MHz
	Lock time	T_{lt}	@ 3.3V/1.1V, FREF=24M,REFDIV=1		250	500	Input clock cycles
	VDDHV current consumption		Fvco = 1000MHz, @3.3V ***Current scale as (Fvco/1GHz)$^{1.5}$***		1.0	1.2	mA
	VDD Current consumption		VDD =1.1V		1.3	1.56	uA/MHz
	Power consumption (power-down mode)		PD=HIGH, @27 ℃		13		uA

Notes:
REFDIV is the input divider value;
FBDIV is the feedback divider value;
POSTDIV is the output divider value

3.6 Electrical Characteristics for USB Interface

Table 3-13 RV1108 Electrical Characteristics for USB Interface

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Transmitter						
High input level	VIH		NA	1.0	NA	V
Low input level	VIL		NA	0	NA	V
Output resistance	ROUT	Classic mode (Vout = 0 or 3.3V)	40.5	45	49.5	ohms
		HS mode (Vout = 0 to 800mV)	40.5	45	49.5	ohms
Output Capacitance	COUT	seen from D+ or D-			3	pF
Output Common Mode Voltage	VM	Classic (LS/FS) mode	1.45	1.65	1.85	V
		HS mode	0.175	0.2	0.225	V
Differential output signal high	VOH	Classic (LS/FS); Io=0mA	2.97	3.3	3.63	V
		Classic (LS/FS); Io=6mA	2.2	0.3	NA	V
		HS mode; Io=0mA	360	400	440	mV
Differential output signal low	VOL	Classic (LS/FS); Io=0mA	-0.33	0	0.33	V
		Classic (LS/FS); Io=6mA	NA	0.3	0.8	V
		HS mode; Io=0mA	-40	0	40	mV
Receiver						
Receiver sensitivity	RSENS	Classic mode		+-250		mV
		HS mode		+-25		mV
Receiver common mode	RCM	Classic mode	0.8	1.65	2.5	V
		HS mode (differential and squelch comparator)	0.1	0.2	0.3	V
		HS mode (disconnect comparator)	0.5	0.6	0.7	V
Input capacitance (seen at D+ or D-)			NA	NA	3	pF
Squelch threshold			100	112	150	mV
Disconnect threshold			570	590	625	mV
High output level	VOH		NA	3.3	NA	V
Low output level	VOL		NA	0	NA	V

3.7 Electrical Characteristics for DDR IO

Table 3-6 RV1108 Electrical Characteristics for DDR IO

Parameters		Symbol	Test condition	Min	Typ	Max	Units
DDR IO @DDR3 mode	Input leakage current, SSTL mode, unterminated		@ 1.5V , 125℃	NA	0		uA
DDR IO @DDR3L mode	Input leakage current		@ 1.35V , 125℃	NA	0	NA	nA

3.8 Electrical Characteristics for eFuse

Table 3-7 RV1108 Electrical Characteristics for eFuse

	Parameters	Symbol	Test condition	Min	Typ	Max	Units
Active mode	VDD current in Read mode	Iread_vdd	nomal read	15	20	30	mA

	VDD current in PGM mode	Ipgm_vdd	STROBE high	0.5	1	2.5	mA
	VQPS current in PGM mode	Ipgm_vqps	STROBE high	5	10	15	mA
standby mode	VDD current in standby mode	Istandby_vdd	Standby	0.2	0.5	2	A

3.9 Electrical Characteristics for HDMI

Table 3-8 RV1108 Electrical Characteristics for HDMI

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Trise and Tfall			<200			ps
Frequency Tolerance, max			-300 ~300			ppm
Clock duty cycle			40%		60%	
Power consumption		1080p		60		mA
Power consumption		2160p		100		mA

3.10 Electrical Characteristics for VDAC

Table 3-9 RV1108 Electrical Characteristics for VDAC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Analog Supply	AVDD		1.62	1.8	1.98	V
Digital Supply	VDD		0.9	1.0	1.1	V
Output Resistance	R_{OUT}			50		KΩ
Output Capacitance	C_{OUT}			10		pF
Full Scale Output Current	I_{OUT}		14.7		34.8	mA
Resistance Load	R_L			75		Ω
Clock Frequency	f_{CLK}				300	MHz
Analog Supply Current	I_{AVDD}	I_{OUT}=14.7mA		18		mA
		I_{OUT}=34.8mA		39		mA
		Power Down		10		uA
Digital Supply Current	I_{VDD}	f_{CLK}=100MHz		100		uA
		Power Down		1		uA

3.11 Electrical Characteristics for TSADC

Table 3-10 RV1108 Electrical Characteristics for TSADC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Temperature Resolution				5		℃
Temperature Range			-40		125	℃
Analog power	I_{AVDD}	Fs= 50KS/s		190		uA
Digital power	I_{VDD}	Fs= 50KS/s		10		uA
Clock Frequency	Fclk	Fclk			800	KHz
Power Down Current from Analog	I_{AVDD}	Power down		1		uA
Power Down Current from Digital	I_{VDD}	Power down		1		uA

3.12 Electrical Characteristics for MIPI DSI

Table 3-11 RV1108 Electrical Characteristics for MIPI DSI

Parameters	Symbol	Test condition	Min	Typ	Max	Units
HS TX static common-mode	Vcmtx		150	200	250	mV
Vcmtx mismatch when output is Differential-1 or Differential-0	ΔVcmtx(1,0)				5	mV
HS Transmit differential voltage	Vod		140	200	270	mV
Vod mismatch when output is Differential-1 or Differential-0	ΔVod				10	mV
HS output high voltage	Vohhs				360	mV
Single ended output impedance	Zos		40	50	62.5	Ohm
Single ended output impedance mismacth	ΔZos				10	%
The venin output high level	Voh		0.9	1	1.1	V
The venin output low level	Vol		-50		50	mV
Output impedance of LP	Zolp		110			Ω
High-level output voltage	Voh		3	3.3		V
Low-level output voltage	Vol			0	0.2	V
Output impedance	Zolp		40		460	Ω
Common-mode variations above 450 MHz	ΔVcmtx(HF)				15	mVrms
Common-mode variations between 50MHz – 450MHz	ΔVcmtx(LF)					mVpeak
20%-80% rise time and fall time	Tr and Tf				0.3	UI
			150			ps
Maximum data rate	Dmax			200		Mbit/s
15%-85% rise time and fall time	Trlp/Tflp		1	1.5	2	ns
Slew rate, transition region	SR		20	27	30	V/ns

3.13 Electrical Characteristics for MIPI CSI

Table 3-12 RV1108 Electrical Characteristics for MIPI CSI

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Common-mode voltage HS receive mode	Vcmrx(dc)		70		300	mV
Differential input high threshold	Vidth				70	mV
Differential input low threshold	Vidtl		-70			mV
Single-ended input high voltage	Vihhs				460	mV
Single-ended input low voltage	Vilhs		-40			mV
Single-ended threshold for HS termination enable	Vterm-en				450	mV
Differential input impedance	Zid		80	100	125	Ω

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Logic 1 input voltage	Vih		880			mV
Logic 0 input voltage, not in ULP state	Vil				550	mV
Logic 0 input voltage, ULP state	Vil-ulps				300	mV
Input hysteresis	Vhyst		25			mV
Common-mode interference beyond 450 MHz	ΔVcmrx(HF)				100	mV
Common-mode interference 50MHz-450MHz	ΔVcmrx(LF)		-50		50	mV
Common-mode termination	Ccm				60	pF
Input pulse rejection	Espike				300	V.ps
Minimum pulse width response	Tmin-rx		20			ns
Peak interference amplitude	Vint				200	mV
Interference frequency	Fint		450			MHz

3.14 Electrical Characteristics for SARADC

Table 3-13 RV1108 Electrical Characteristics for SARADC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Analog Supply	AVDD		1.62	1.8	1.98	V
Digital Supply	VDD		0.9	1.0	1.1	V
Effective Number of Bit	ENOB			9		Bit
Differential Nonlinearity	DNL		-1		+1	LSB
Integral Nonlinearity	INL		-2		+2	LSB
Input Voltage Range	Vin		0		1	AVDD
Input Capacitance	Cin			10		pF
Sampling rate	fs				1	MS/s
Spurious Free Dynamic Range	SFDR	Fs=1MS/s Fout=1.17KHz		61		dB
Signal to Noise and Harmonic Ratio	SNDR			56		dB
Analog Supply Current	I_{AVDD}	Fs=1MS/s		450		uA
		Power Down		1		uA
Digital Supply Current	I_{VDD}	Fs=1MS/s		50		uA
		Power Down		1		uA

3.15 Electrical Characteristics for ACODEC

Table 3-14 RV1108 Electrical Characteristics for ACODEC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Analog Supply	AVDD		1.62	1.8	1.98	V

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Digital Supply	DVDD		0.9	1.0	1.1	V
Bias Voltage	V_{MICB}		0.5 * AVDD		0.85 * AVDD	V
Bias Voltage	I_{MICB}				3	mA
Programmable Gain	G_{BST}		0		20	dB
Input Resistance	R_{IN}	G_{BST}=0dB		110		KΩ
		G_{BST}=20dB		20		KΩ
Input Capacitance	C_{IN}			10		pF
Programmable Gain	G_{ALC}		-18		28.5	dB
Signal to Noise Ratio	SNR	A-weighted		92		dB
Total Harmonic Distortion	THD	-3dBFS input		-81		dB
Programmable Gain	G_{DRV}		-39		6	dB
Output Resistance	R_{OUT}			1		Ω
Output Capacitance	C_{OUT}			20		pF
Power Supply Rejection	PSRR	1KHz		70		dB
Signal to Noise Ration	SNR	A-weighted		93		dB
Total Harmonic Distortion	THD	-3dBFS output 600Ω load		-80		dB

3.16 Electrical Characteristics for VIDEO ADC

Table 3-15 RV1108 Electrical Characteristics for VIDEO ADC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Max Current	I_{max}			800		uA
Min Current	I_{min}			50		uA
Current Consumption	I_{sup}			1		uA
Total Harmonic Distortion AGC setting 101010=0dB Vin : mV_{pp}	THD_N	F_{sig}=5.5MHZ		-72	-65	dB
		F_{sig}=5.5MHZ		-61	-56	dB
		F_{sig}=88MHZ		-60	-49	dB
BW in bypass	BW_{bp}			200	100	MHz
Output noise	N_{int}			725		uV
Current Consumption	I_{buff}			9.4		mA
	I_{agc}			4.25		mA
	I_{filter}			4.25		mA
Total Power Consumption	I_{sup}			18		mA
Resolution	Res			10		Bit
Sampling Frequency	Fs			50	60	MHz
Input Voltage for Full Scale	V_{in}			1		V_{pp}

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Input Common Mode	V_{CM}			0.5		V
Differential Input Capacitance	C_{in_diff}			2		pF
Single ended input capacitance	C_{in_cm}			3		pF
Current Consumption	I_{sup}	V_{dd}=1.1V		45		mA

Chapter 4 Thermal Management

4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature of RV1108A, RV1108G and RV1108K1 has to be below 125℃.

4.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package used on RV1108A, RV1108G and RV1108K1. The resulting simulation data for reference only, please prevail in kind test.

Table 4-1 Thermal Resistance Characteristics

Package (BGA359)	**Power(W)**	$\boldsymbol{\theta_{JA}}$(℃/$\boldsymbol{W}$)	$\boldsymbol{\theta_{JB}}$(℃/$\boldsymbol{W}$)	$\boldsymbol{\theta_{JC}}$(℃/$\boldsymbol{W}$)
RV1108A	2.2	16.37	10.25	7.63
RV1108G	2.518	15.62	8.78	7.18
RV1108K1	2.2	16.37	10.25	7.63

Note: The testing PCB is base on 4 layers, 14mmx 14mm, 1.1 mm Thickness, Ambient temperature is 25.3° C.

