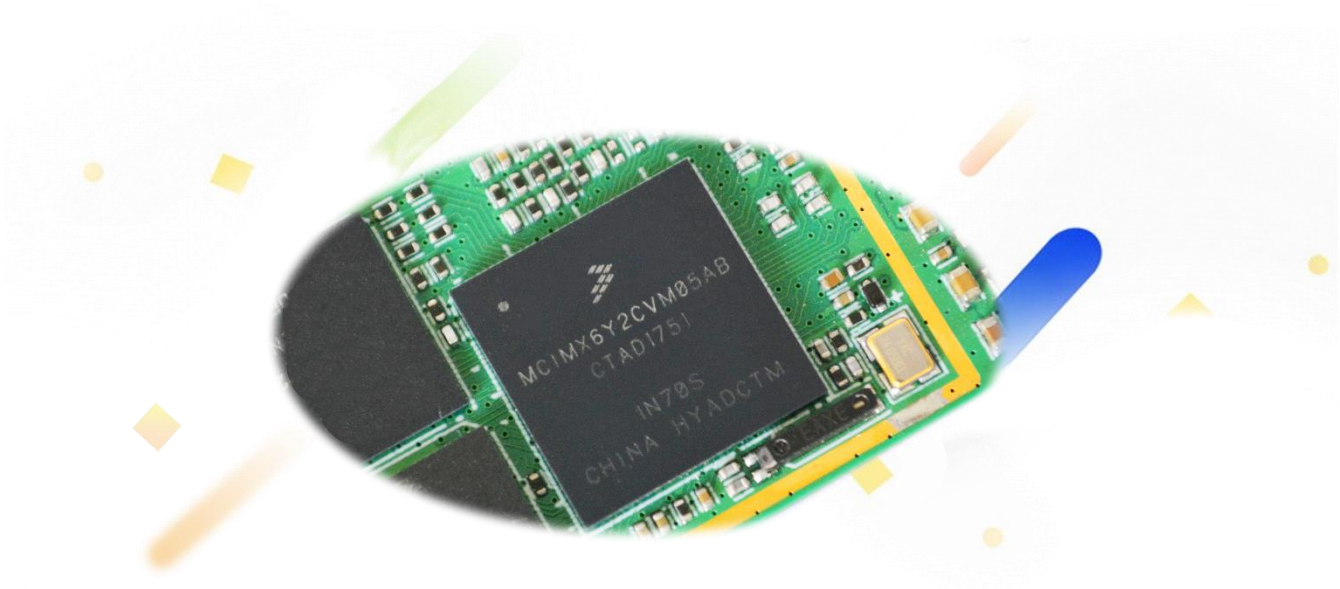
CM6ULL Reference User Manual

V2.202002



Boardcon Embedded Design

www.armdesigner.com

1. Introduction

1.1. About this Manual

This manual is intended to provide the user with an overview of the board and benefits, complete features specifications, and set up procedures. It contains important safety information as well.

1.2. Feedback and Update to this Manual

To help our customers make the most of our products, we are continually making additional and updated resources available on the Boardcon website (www.boardcon.com , www.armdesigner.com).

These include manuals, application notes, programming examples, and updated software and hardware. Check in periodically to see what's new!

When we are prioritizing work on these updated resources, feedback from customers is the number one influence, If you have questions, comments, or concerns about your product or project, please no hesitate to contact us at support@armdesigner.com.

1.3. Limited Warranty

Boardcon warrants this product to be free of defects in material and workmanship for a period of one year from date of buy. During this warranty period Boardcon will repair or replace the defective unit in accordance with the following process:

A copy of the original invoice must be included when returning the defective unit to Boardcon. This limited warranty does not cover damages resulting from lighting or other power surges, misuse, abuse, abnormal conditions of operation, or attempts to alter or modify the function of the product.

This warranty is limited to the repair or replacement of the defective unit. In no event shall Boardcon be liable or responsible for any loss or damages, including but not limited to any lost profits, incidental or consequential damages, loss of business, or anticipatory profits arising from the use or inability to use this product.

Repairs make after the expiration of the warranty period are subject to a repair charge and the cost of return shipping. Please contact Boardcon to arrange for any repair service and to obtain repair charge information.

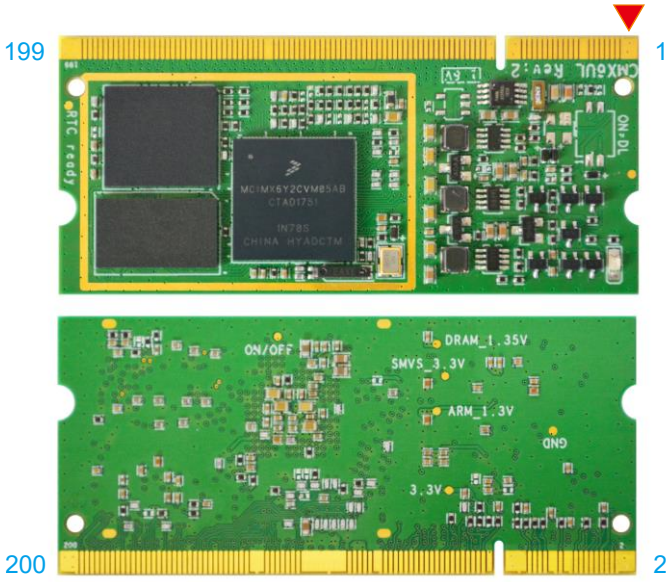
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1 CM6ULL Introduction

1.1 Summary

The CM6ULL is a highly flexible System-on-Module (SoM) based on NXP/Freescale's i.MX 6ULL ARM Cortex-A7™ processor. The small and energy-efficient ARM-based module provides maximum performance in low-power, space constrained embedded environments. It is designed specifically for Electronics Point-of-Sale device, Telematics, IoT Gateway, Access control panels, Human Machine Interfaces (HMI) and Smart appliances.



1.2 Processor Features

SPECIFICATIONS	
CPU	Cortex-A7 core @528MHz, 128 KB L2 cache
Memory	• 16-bit LP-DDR2, DDR3/DDR3L • 8/16-bit Parallel NOR FLASH / PSRAM • Dual-channel Quad-SPI NOR FLASH • 8-bit Raw NAND FLASH with 40-bit ECC
Display	• Parallel LCD Display up to WXGA (1366x768) • 8/10/16/24-bit Parallel Camera Sensor Interface • Electrophoretic display controller supports direct-driver for E-Ink EPD panel, with up to 2048x1536 resolution at 106 Hz
Power Management	Partial PMU Integration

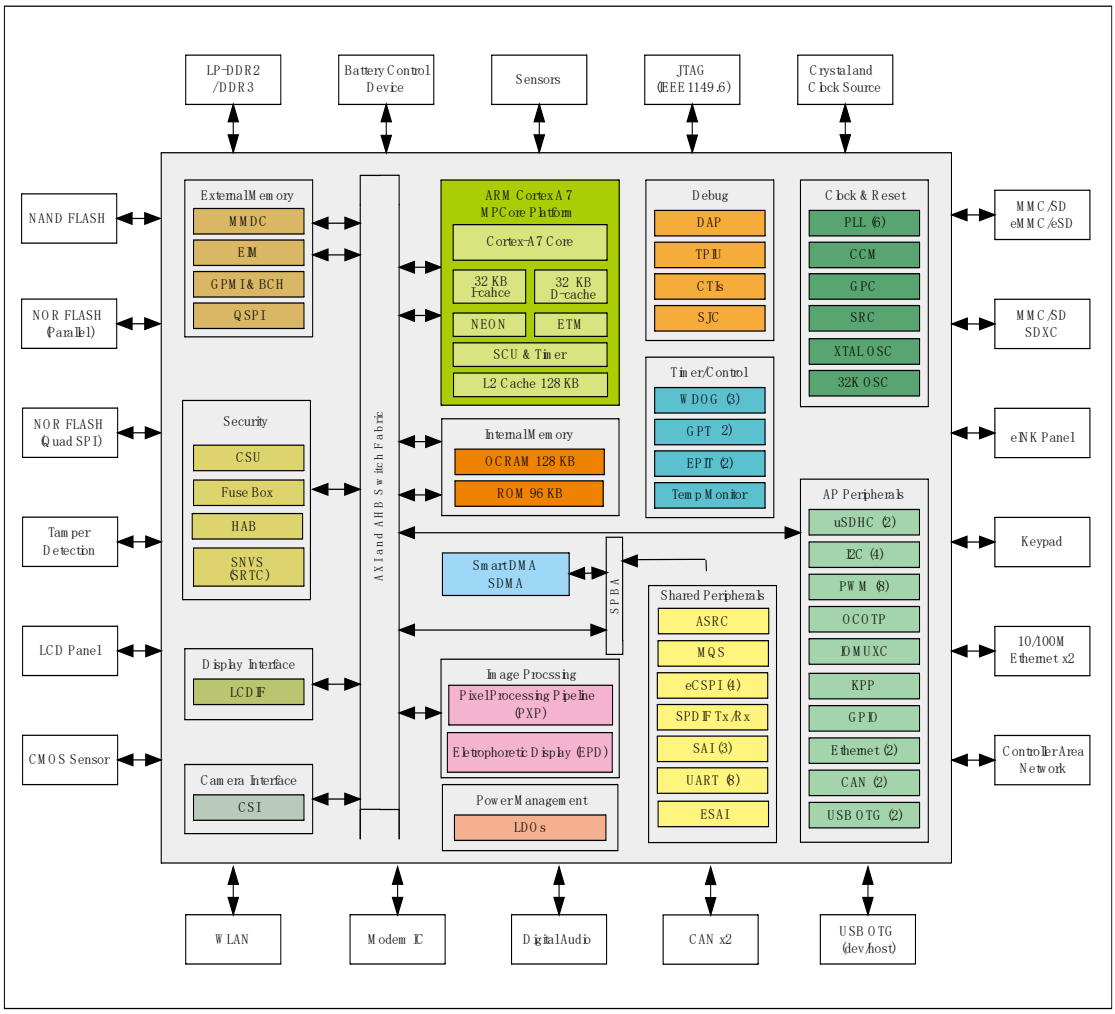
Audio	3x I2S/SAI, S/PDIF Tx/Rx
MMC/SD/SDIO	2x MMC 4.5/SD 3.0/SDIO Port
USB	2x USB 2.0 OTG, HS/FS, Device or Host with PHY
Security	Security Block: TRNG, Crypto Engine (AES with DPA, TDES/SHA/RSA), Secure Boot
Ethernet	2x 10/100 Ethernet with IEEE 1588
Temperature	0°C to +95°C

1.3 SoM Specifications

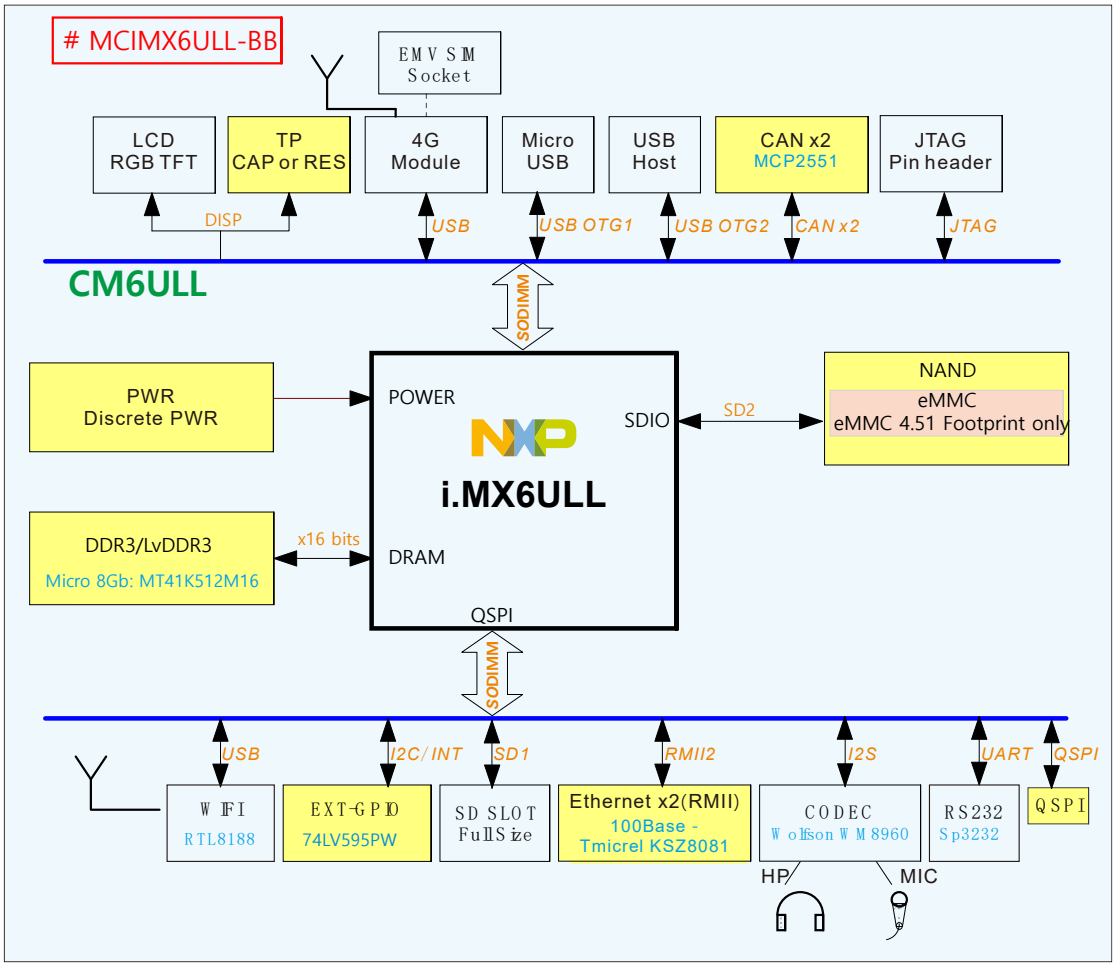
Feature	Specifications
CPU	NXP i.MX 6ULL ARM Cortex-A7™ @ 528MHz
Memory	512MB DDR3L
Flash	4GB eMMC
Power	5V
Pin out	USB OTG, UART, HDMI, LCD, Audio I/O, Ethernet (10/100T), MMC/SD/SDIO, Camera, JTAG, PWM, GPIO
Layer	4 layers
Connector	200-pin SO-DIMM edge connector
Dimension	67.7mm x 30.0 mm

1.4 Block Diagram

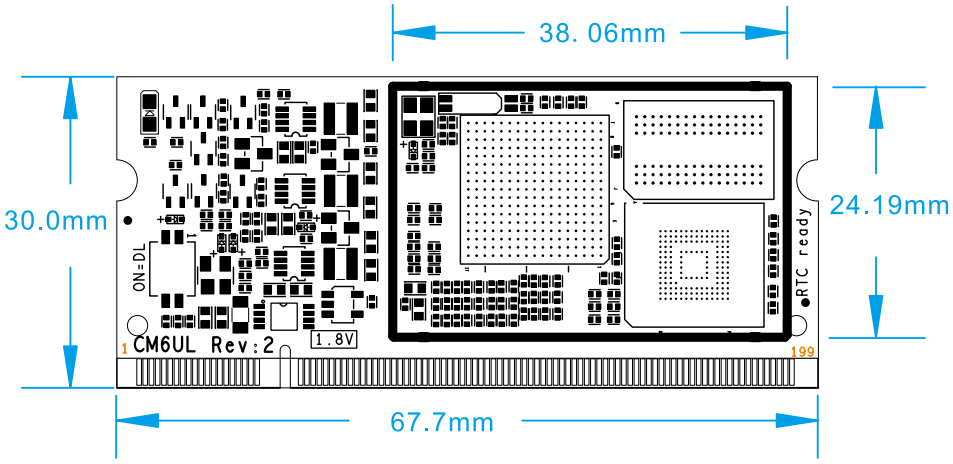
1.4.1 i.MX 6ULL Block Diagram



1.4.2 Evaluation Kit Block Diagram



1.5 PCB Dimension



1.6 Pin Definition

Front side Back side

Pin	Signal	Description	IO Voltage
1	GND	Ground	0V
2	GND	Ground	0V
3	PMIC_STBY_REQ	When the processor enters SUSPEND mode, it will assert this signal.	3.3V
4	MX6_POR_B	Processor reset single	3.3V
5	PMIC_ON_REQ	Active high power-up request output from iMX6UL SoC	3.3V
6	NC		
7	BOOT_MODE1	BOOT MODE1	3.3V
8	VDD_COIN_3V	COIN battery power	3.0V
9	BOOT_MODE0	BOOT MODE0	3.3V
10	SNVS_TAMPER9	Secure Non-Volatile Storage tamper	3.3V
11	USB_OTG2_VBUS	USB2 OTG VBUS	5.0V
12	SNVS_TAMPER5	Secure Non-Volatile Storage tamper	3.3V
13	USB_OTG1_VBUS	USB1 OTG VBUS	3.3V
14	ON/OFF	PMC ON/OFF switch	3.3V
15	GND	Ground	0V
16	POR_B	Power on reset	3.3V
17	GND	Ground	0V
18	SNVS_TAMPER8	Secure Non-Volatile Storage tamper	3.3V
19	USB_OTG2_DP	USB2 data positive	3.3V
20	GND	Ground	0V
21	USB_OTG2_DN	USB2 data negative	3.3V
22	GND	Ground	0V
23	GND	Ground	0V
24	SNVS_TAMPER7	Secure Non-Volatile Storage tamper	3.3V
25	USB_OTG1_DP	USB1 data positive	3.3V
26	GND	Ground	0V
27	USB_OTG1_DN	USB1 data negative	3.3V
28	GND	Ground	0V
29	GND	Ground	0V
30	SNVS_TAMPER4	Secure Non-Volatile Storage tamper	3.3V
31	NC		
32	SNVS_TAMPER1	Secure Non-Volatile Storage tamper	3.3V
33	SPDIF_TX/ spdif.OUT	Sony/Philips Digital Interface OUT	3.3V
34	SNVS_TAMPER3	Secure Non-Volatile Storage tamper	3.3V
35	GND	Ground	0V
36	SNVS_TAMPER0	Secure Non-Volatile Storage tamper	3.3V

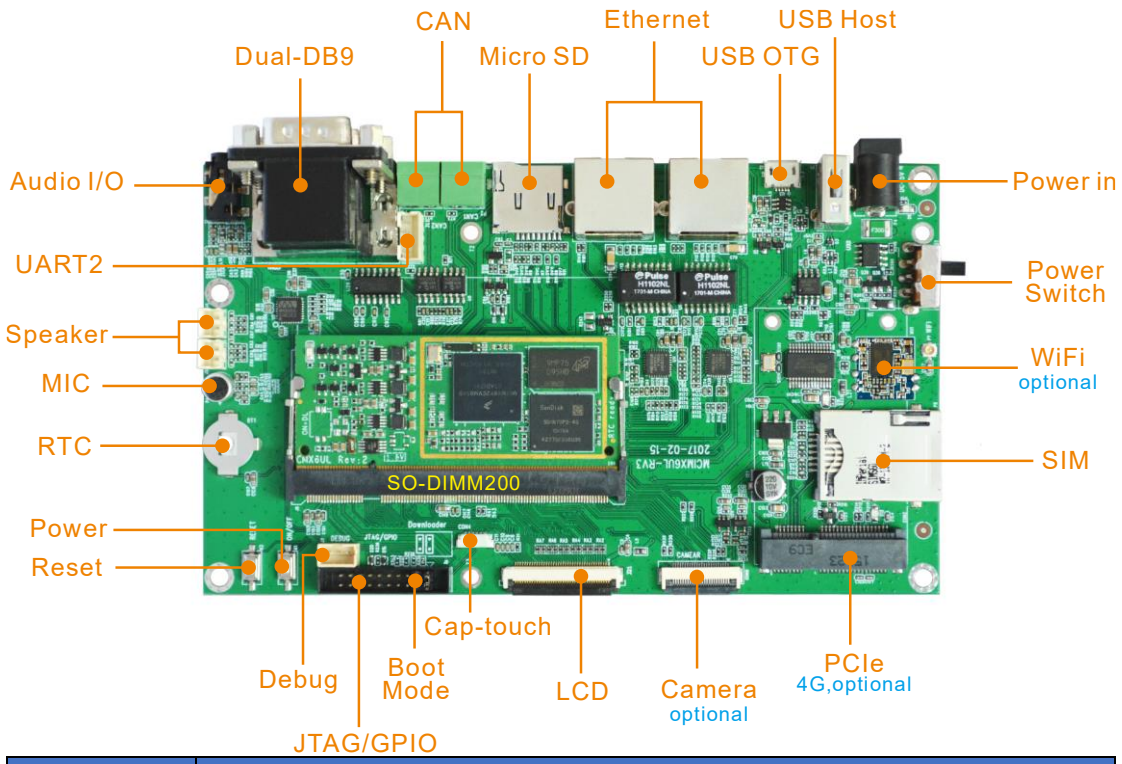
Pin	Signal	Description	IO Voltage
37	NC		
38	GND	Ground	0V
39	RTC_CLKOUT	RTC clock output	3.3V
40	GND	Ground	0V
41	GND	Ground	0V
42	SNVS_TAMPER6	Secure Non-Volatile Storage tamper	3.3V
43	JTAG_TDI	JTAG data in	3.3V
44	SNVS_TAMPER2	Secure Non-Volatile Storage tamper	3.3V
45	BLT_PWM	Backlight PWM	3.3V
46	JTAG_TMS	JTAG mode select	3.3V
47	USB_OTG1_PWR	USB OTG power	3.3V
48	JTAG_nTRST	JTAG reset	3.3V
49	SD1_VSELECT	SD Voltage select	3.3V
50	GND	Ground	0V
51	GND	Ground	0V
52	JTAG_TDO	JTAG data output	3.3V
53	ENET_MDC	Ethernet Management Clock Reference	3.3V
54	JTAG_TCK	JTAG clock	3.3V
55	USB_OTG2_OC	USB OTG over-current	3.3V
56	SD1_nRST	SD1 card reset	3.3V
57	UART1_TXD	UART1 output	3.3V
58	USB_OTG2_PWR	USB OTG power	3.3V
59	GND	Ground	0V
60	GND	Ground	0V
61	ENET_MDIO	Ethernet Management Data I/O	3.3V
62	USB_OTG1_OC	USB OTG over-current	3.3V
63	UART1_RXD	UART1 input	3.3V
64	USB_OTG1_ID	USB1_OTG_ID	3.3V
65	UART2_TXD	UART2 output	3.3V
66	UART1_CTS	UART1 Clear to Send	
67	UART2_RXD	UART2 input	3.3V
68	UART5_RXD	UART5 input	3.3V
69	UART3_TXD	UART3 output	3.3V
70	GND	Ground	0V
71	GND	Ground	0V
72	UART2_CTS	UART2 Clear to Send	3.3V
73	UART3_RXD	UART3 input	3.3V
74	UART1_RTS	UART1 Request to Send	3.3V
75	UART4_TXD	UART4 output	3.3V
76	UART3_CTS	UART3 Clear to Send	3.3V
77	UART4_RXD	UART4 input	3.3V
78	UART2_RTS	UART2 Request to Send	3.3V

Pin	Signal	Description	IO Voltage
79	UART5_TXD	UART5 output	3.3V
80	UART3_RTS	UART3 Request to Send	3.3V
81	GND	Ground	0V
82	GND	Ground	0V
83	NC		
84	GND	Ground	0V
85	VEXT_3V3	Output to baseboard 3.3V	3.3V
86	NC		
87	VEXT_3V3	Output to baseboard 3.3V	3.3V
88	VEXT_3V3	Output to baseboard 3.3V	3.3V
89	VEXT_3V3	Output to baseboard 3.3V	3.3V
90	VEXT_3V3	Output to baseboard 3.3V	3.3V
91	VEXT_3V3	Output to baseboard 3.3V	3.3V
92	VEXT_3V3	Output to baseboard 3.3V	3.3V
93	VEXT_3V3	Output to baseboard 3.3V	3.3V
94	NC		
95	NC		
96	VSYS	POWER input	5V
97	ENET1_RXD0	Ethernet1 input data0	3.3V
98	VSYS	POWER input	5V
99	ENET1_RXD1	Ethernet1 input data1	3.3V
100	VSYS	POWER input	5V
101	ENET1_CRS_DV	Ethernet1 input enable	3.3V
102	VSYS	POWER input	5V
103	GND	Ground	0V
104	VSYS	POWER input	5V
105	ENET2_TX_CLK	Ethernet2 output clock	3.3V
106	VSYS	POWER input	5V
107	GND	Ground	0V
108	VSYS	POWER input	5V
109	ENET2_RXER	Ethernet2 input enable	3.3V
110	VSYS	POWER input	5V
111	ENET2_RXD0	Ethernet2 input data0	3.3V
112	VSYS	POWER input	5V
113	ENET2_RXD1	Ethernet2 input data1	3.3V
114	ENET1_TXEN	Ethernet1 output enable	3.3V
115	GND	Ground	0V
116	GND	Ground	0V
117	ENET2_CRS_DV	Ethernet2 input enable	3.3V
118	ENET1_TX_CLK	Ethernet1 output clock	3.3V
119	ENET2_TXD1	Ethernet2 output data1	3.3V
120	GND	Ground	0V

Pin	Signal	Description	IO Voltage
121	ENET2_TXEN	Ethernet2 output enable	0V
122	ENET1_TXD0	Ethernet1 output data0	3.3V
123	ENET2_TXD0	Ethernet2 output data0	3.3V
124	ENET1_TXD1	Ethernet1 output data1	3.3V
125	GND	Ground	0V
126	ENET1_RXER	Ethernet1 input enable	3.3V
127	GND	Ground	0V
128	GND	Ground	0V
129	LCD_DATA21	LCD DATA21	3.3V
130	GND	Ground	0V
131	LCD_DATA22	LCD DATA22	3.3V
132	GND	Ground	0V
133	LCD_DATA17	LCD DATA17	3.3V
134	LCD_DATA23	LCD DATA23	3.3V
135	GND	Ground	0V
136	GND	Ground	0V
137	LCD_DATA18	LCD DATA18	3.3V
138	LCD_DATA19	LCD DATA19	3.3V
139	LCD_DATA13	LCD DATA13	3.3V
140	LCD_DATA20	LCD DATA20	3.3V
141	LCD_DATA14	LCD DATA14	3.3V
142	LCD_DATA15	LCD DATA15	3.3V
143	LCD_DATA8	LCD DATA8	3.3V
144	LCD_DATA16	LCD DATA16	3.3V
145	LCD_DATA9	LCD DATA9	3.3V
146	GND	Ground	0V
147	GND	Ground	0V
148	LCD_DATA11	LCD DATA11	3.3V
149	LCD_DATA5	LCD DATA5	3.3V
150	LCD_DATA12	LCD DATA12	3.3V
151	LCD_DATA6	LCD DATA6	3.3V
152	LCD_DATA10	LCD DATA10	3.3V
153	LCD_DATA0	LCD DATA0	3.3V
154	LCD_DATA3	LCD DATA3	3.3V
155	LCD_DATA1	LCD DATA1	3.3V
156	GND	Ground	0V
157	LCD_RST	LCD reset	3.3V
158	LCD_DATA4	LCD DATA4	3.3V
159	GND	Ground	0V
160	LCD_HSYNC	LCD Horizontal Sync	3.3V
161	LCD_PCLK	LCD Pixel Clock	3.3V
162	LCD_VSYNC	LCD Vertical Sync	3.3V

Pin	Signal	Description	IO Voltage
163	LCD_DE	LCD Data Enable	3.3V
164	LCD_DATA2	LCD DATA2	3.3V
165	GND	Ground	0V
166	LCD_DATA7	LCD DATA7	3.3V
167	SD1_DATA0	SD1 DATA0	3.3V
168	GND	Ground	0V
169	SD1_DATA3	SD1 DATA3	3.3V
170	QSPIA_nSS0	QSPIA chip select0	3.3V
171	SD1_DATA1	SD1 DATA1	3.3V
172	QSPIA_DATA0	QSPIA DATA0	3.3V
173	SD1_CMD	SD1 command	3.3V
174	QSPIA_DATA3	QSPIA DATA3	3.3V
175	SD1_DATA2	SD1 DATA2	3.3V
176	QSPIA_DATA2	QSPIA DATA2	3.3V
177	GND	Ground	0V
178	QSPIA_DATA1	QSPIA DATA1	3.3V
179	SD1_CLK	SD1 clock	3.3V
180	GND	Ground	0V
181	GND	Ground	0V
182	QSPIA_SCLK	QSPIA clock	3.3V
183	CSI_PIXCLK	CSI Pixel Clock	3.3V
184	GND	Ground	0V
185	GND	Ground	0V
186	CSI_DATA6	CSI DATA6	3.3V
187	CSI_MCLK	CSI Main clock	3.3V
188	CSI_DATA7	CSI DATA7	3.3V
189	GND	Ground	0V
190	CSI_DATA5	CSI DATA5	3.3V
191	CSI_DATA4	CSI DATA4	3.3V
192	CSI_DATA3	CSI DATA3	3.3V
193	CSI_DATA1	CSI DATA1	3.3V
194	CSI_DATA2	CSI DATA2	3.3V
195	CSI_DATA0	CSI DATA0	3.3V
196	NVCC_CSI	CSI interface power	3.3V
197	CSI_HSYNC	CSI Horizontal Sync	3.3V
198	CSI_VSYNC	CSI Vertical Hold	3.3V
199	GND	Ground	0V
200	GND	Ground	0V

1.7 EM6ull EVK



Feature	Specifications
CPU	NXP i.MX 6ULL Cortex-A7 @528MHz
RAM	512MB DDR3L
storage	4GB eMMC
Serial Port	1x 3pin debug serial port; 1x 4pin UART; 2x DB9 UARTs.
LCD	40pin FPC, 6pin Capacitive touch screen connector. Support 4.3-/7-inch Res- touch screen, 4.3-inch Cap-touch screen.
USB	1x USB2.0 OTG, 1x USB2.0 Host
GPIO	1x 20Pin header. The functions include JTAG, QSPI and Boot mode selection.
Audio	WM8960G chip. 3.5 mm audio stereo headset, support Audio in/out; L/R speaker connectors; Board-mounted microphone
SD	On-board 1x Micro SD card slot(baseboard), and the eMMC on the CPU board can be replaced by Micro SD slot
Ethernet	2x 10/100 Mbit/s Ethernet, RJ45 connector. KSZ8081RNBCA controller
WiFi	On-board WiFi module(optional), Realtek RTL8188EUS.
Camera	24pin FPC connector.

4G	MINI PCI-E connector. EC20 model
Switch	1x Power switch
Buttons	Reset, ON/OFF (software)
Dimension	90 x 155mm

2 Peripheral Introduction

Some pins are multifunctional. Pin function selection is controlled by software. Each pin can be used for a single function at a time.

2.1 Display

The CMX6ULL provides one parallel LCD interface on the SODIMM connector.

Features

- Up to 1366x768 resolution at 60Hz
- Up to 24-bit color (18-bit recommended)
- Supports parallel TTL displays and smart displays
- Max pixel clock 85MHz

Signal	Description	Pin	Defaults Function
LCD_DATA0	LCD data0	153	LCD_DATA0
LCD_DATA1	LCD data1	155	LCD_DATA1
LCD_DATA2	LCD data2	164	LCD_DATA2
LCD_DATA3	LCD data3	154	LCD_DATA3
LCD_DATA4	LCD data4	158	LCD_DATA4
LCD_DATA5	LCD data5	149	LCD_DATA5
LCD_DATA6	LCD data6	151	LCD_DATA6
LCD_DATA7	LCD data7	166	LCD_DATA7
LCD_DATA8	LCD data8	143	LCD_DATA8
LCD_DATA9	LCD data9	145	LCD_DATA9
LCD_DATA10	LCD data10	152	LCD_DATA10
LCD_DATA11	LCD data11	148	LCD_DATA11
LCD_DATA12	LCD data12	150	LCD_DATA12
LCD_DATA13	LCD data13	139	LCD_DATA13
LCD_DATA14	LCD data14	141	LCD_DATA14
LCD_DATA15	LCD data15	142	LCD_DATA15
LCD_DATA16	LCD data16	144	LCD_DATA16

Signal	Description	Pin	Defaults Function
LCD_DATA17	LCD data17	133	LCD_DATA17
LCD_DATA18	LCD data18	137	LCD_DATA18
LCD_DATA19	LCD data19	138	LCD_DATA19
LCD_DATA20	LCD data20	140	LCD_DATA20
LCD_DATA21	LCD data21	129	LCD_DATA21
LCD_DATA22	LCD data22	131	LCD_DATA22
LCD_DATA23	LCD data23	134	LCD_DATA23
LCD_DE	LCD Data Enable	163	LCD_DE
LCD_HSYNC	LCD Horizontal Sync	160	LCD_HSYNC
LCD_VSYNC	LCD Vertical Sync	162	LCD_VSYNC
LCD_PCLK	LCD Pixel Clock	161	LCD_PCLK

2.2 Camera I/F

The i.MX 6ULL CSI IP provides parallel CSI standard camera interface port.

Features

- up to 24 bit and 133.3 MHz pixel clock
- Support for CCIR656 (BT.656)
- 8/10/16/24-bit parallel video interface

Signal	Description	Pin	Defaults Function
CSI_DATA0	CSI DATA0	195	CSI_DATA0
CSI_DATA1	CSI DATA1	193	CSI_DATA1
CSI_DATA2	CSI DATA2	194	CSI_DATA2
CSI_DATA3	CSI DATA3	192	CSI_DATA3
CSI_DATA4	CSI DATA4	191	CSI_DATA4
CSI_DATA5	CSI DATA5	190	CSI_DATA5
CSI_DATA6	CSI DATA6	186	CSI_DATA6
CSI_DATA7	CSI DATA7	188	CSI_DATA7
CSI_HSYNC	CSI Horizontal Sync	197	CSI_HSYNC
CSI_VSYNC	CSI Vertical Sync	198	CSI_VSYNC
CSI_MCLK	CSI Main clock	187	CSI_MCLK
CSI_PIXCLK	CSI Pixel Clock	183	CSI_PIXCLK

2.3 Audio

2.3.1 SAI

SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces. i.MX 6ULL features 3x SAI. An external audio codec can be placed on the carrier board to achieve higher quality audio.

Signal	Description	Pin	Defaults Function
sai1.MCLK	sai1 Master Clock	193	CSI_DATA1
sai1.TX_SYNC	sai1 Transmit Frame Sync	191	CSI_DATA4
sai1.TX_BCLK	sai1 Transmit Clock	190	CSI_DATA5
sai1.TX_DATA	sai1 Data Transmit	188	CSI_DATA7
sai1.RX_SYNC	sai1 Receive Frame Sync	194	CSI_DATA2
sai1.RX_BCLK	sai1 Receive Clock	192	CSI_DATA3
sai1.RX_DATA	sai1 Data Receive	186	CSI_DATA6
sai2.MCLK	sai2 Master Clock	46	JTAG_TMS
		179	SD1_CLK
sai2.TX_SYNC	sai2 Transmit Frame Sync	52	JTAG_TDO
		167	SD1_DATA0
sai2.TX_BCLK	sai2 Transmit Clock	43	JTAG_TDI
		171	SD1_DATA1
sai2.TX_DATA	sai2 Data Transmit	169	SD1_DATA3
sai2.RX_SYNC	sai2 Receive Frame Sync	173	SD1_CMD
sai2.RX_DATA	sai2 Data Receive	54	JTAG_TCK
		175	SD1_DATA2
sai3.MCLK	sai3 Master Clock	145	LCD_DATA9
		161	LCD_PCLK
sai3.TX_SYNC	sai3 Transmit Frame Sync	150	LCD_DATA12
		163	LCD_DE
sai3.TX_BCLK	sai3 Transmit Clock	139	LCD_DATA13
		160	LCD_HSYNC
sai3.TX_DATA	sai3 Data Transmit	142	LCD_DATA15
sai3.RX_SYNC	sai3 Receive Frame Sync	152	LCD_DATA10
sai3.RX_BCLK	sai3 Receive Clock	148	LCD_DATA11
sai3.RX_DATA	sai3 Data Receive	141	LCD_DATA14
		162	LCD_VSYNC

2.3.2 SPDIF

Sony Philips Digital Interconnect Format (SPDIF).

Features

- Internal data width: 24-bit
- Left and right channel 16x24-bit FIFO (receive and transmit)

Signal	Description	Pin	Defaults Function
SPDIF_TX/ spdif.OUT	Serial data output	33	SPDIF_TX
		45	BLT_PWM
spdif.IN	Serial data input	56	SD1_nRST
		143	LCD_DATA8
		179	SD1_CLK

2.4 Ethernet

CM6UL supports two Ethernet (10/100T) connectors.

Features

- 10/100 Mbit/s Ethernet/IEEE 802.3 networks
- support the IEEE 1588 standard.

Signal	Description	Pin	Defaults Function
ENET1_TXD0	Ethernet1 output data0	122	ENET1_TXD0
ENET1_TXD1	Ethernet1 output data1	124	ENET1_TXD1
ENET1_TXEN	Ethernet1 output enable	114	ENET1_TXEN
ENET1_TX_CLK	Ethernet1 output clock	118	ENET1_TX_CLK
ENET1_RXD0	Ethernet1 input data0	97	ENET1_RXD0
ENET1_RXD1	Ethernet1 input data1	99	ENET1_RXD1
ENET1_RXER	Ethernet1 input enable	126	ENET1_RXER
ENET1_CRS_DV	Ethernet1 input enable	101	ENET1_CRS_DV
ENET2_TXD0	Ethernet2 output data0	123	ENET2_TXD0
ENET2_TXD1	Ethernet2 output data1	119	ENET2_TXD1
ENET2_TXEN	Ethernet2 output enable	121	ENET2_TXEN
ENET2_TX_CLK	Ethernet2 output clock	105	ENET2_TX_CLK
ENET2_RXD0	Ethernet2 input data0	111	ENET2_RXD0
ENET2_RXD1	Ethernet2 input data1	113	ENET2_RXD1
ENET2_RXER	Ethernet2 input enable	109	ENET2_RXER
ENET2_CRS_DV	Ethernet2 input enable	117	ENET2_CRS_DV

2.5 USB

Two USB controllers and PHYs that support USB 2.0 and OTG. Each USB instance contains USB 2.0 core, which can operate in 2.0 mode.

Signal	Description	Pin	Defaults Function
USB_OTG1_DN	USB1 data negative	27	USB_OTG1_DN
USB_OTG1_DP	USB1 data positive	25	USB_OTG1_DP
USB_OTG1_VBUS	USB1 OTG VBUS	13	USB_OTG1_VBUS
USB_OTG1_ID	USB1_OTG_ID	64	USB_OTG1_ID
USB_OTG2_DN	USB2 data negative	21	USB_OTG2_DN
USB_OTG2_DP	USB2 data positive	19	USB_OTG2_DP
USB_OTG2_VBUS	USB2 OTG VBUS	11	USB_OTG2_VBUS

2.6 SD/SDIO

The i.MX 6ULL SoC provides two SD/SDIO interfaces. One interface is available as standard interface,

the other is available on the module edge connector pin as an alternate function if there isn't WiFi module. This secondary interface can be used with up to 8 data bits while the standard interface is only available with 4-bit.

Two MMC/SD/SDIO card ports all supporting:

- 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR-104 mode (104 MB/s max)
- 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max)
- 4-bit or 8-bit transfer

Signal	Description	Pin	Defaults Function
SD1_CLK	SD1 clock	179	SD1_CLK
SD1_CMD	SD1 Command	173	SD1_CMD
SD1_CD	SD1 Card Detect	74	UART1_RTS
SD1_DATA0	SD1 DATA	167	SD1_DATA0
SD1_DATA1	SD1 DATA	171	SD1_DATA1
SD1_DATA2	SD1 DATA	175	SD1_DATA2
SD1_DATA3	SD1 DATA	169	SD1_DATA3
usdhc1.DATA4	uSDHC1 data	172	QSPIA_DATA0
usdhc1.DATA5	uSDHC1 data	178	QSPIA_DATA1
usdhc1.DATA6	uSDHC1 data	176	QSPIA_DATA2
usdhc1.DATA7	uSDHC1 data	174	QSPIA_DATA3
usdhc2.CLK	uSDHC2 clock	198	CSI_VSYNC
usdhc2.CMD	uSDHC2 command	197	CSI_HSYNC
usdhc2.DATA0	uSDHC2 data	195	CSI_DATA0
usdhc2.DATA1	uSDHC2 data	193	CSI_DATA1
usdhc2.DATA2	uSDHC2 data	194	CSI_DATA2
usdhc2.DATA3	uSDHC2 data	192	CSI_DATA3
usdhc2.DATA4	uSDHC2 data	191	CSI_DATA4
usdhc2.DATA5	uSDHC2 data	190	CSI_DATA5
usdhc2.DATA6	uSDHC2 data	186	CSI_DATA6
usdhc2.DATA7	uSDHC2 data	188	CSI_DATA7

2.7 SPI

The i.MX 6ULL provides four eCSPI (Enhanced CSPI), up to 52 Mbps each, and one Quad SPI to connect to serial NOR flash

2.8.1 ECSPI

Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.

Signal	Description	Pin	Defaults Function
ecspi1.SCLK	ecspi1 Serial Clock	140	LCD_DATA20
		191	CSI_DATA4
ecspi1.SS0	ecspi1 Slave Select	129	LCD_DATA21
		190	CSI_DATA5
ecspi1.MOSI	ecspi1 Master Output, Slave Input	131	LCD_DATA22
		186	CSI_DATA6
ecspi1.MISO	ecspi1 Master Input, Slave Output	134	LCD_DATA23
		188	CSI_DATA7
ecspi2.SCLK	ecspi2 Serial Clock	195	CSI_DATA0
ecspi2.SS0	ecspi2 Slave Select	193	CSI_DATA1
ecspi2.MOSI	ecspi2 Master Output, Slave Input	194	CSI_DATA2
ecspi2.MISO	ecspi2 Master Input, Slave Output	192	CSI_DATA3
ecspi3.SCLK	ecspi3 Serial Clock	178	QSPIA_DATA1
ecspi3.SS0	ecspi3 Slave Select	172	QSPIA_DATA0
ecspi3.MOSI	ecspi3 Master Output, Slave Input	176	QSPIA_DATA2
ecspi3.MISO	ecspi3 Master Input, Slave Output	174	QSPIA_DATA3
ecspi4.SS0	ecspi4 Slave Select	109	ENET2_RXER
ecspi4.MOSI	ecspi4 Master Output, Slave Input	121	ENET2_TXEN
ecspi4.MISO	ecspi4 Master Input, Slave Output	105	ENET2_TX_CLK

2.8.2 QSPI

Quad SPI module acts as an interface to external serial flash devices. This module contains the following features:

- Flexible sequence engine to support various flash vendor devices
- Single pad/Dual pad/Quad pad mode of operation
- Single Data Rate/Double Data Rate mode of operation
- Parallel Flash mode
- DMA support
- Memory mapped read access to connected flash devices
- Multi-master access with priority and flexible and configurable buffer for each master

Signal	Description	Pin	Defaults Function
QSPIA_SCLK	QSPIA clock	182	QSPIA_SCLK
QSPIA_nSS0	QSPIA chip select0	170	QSPIA_nSS0
QSPIA_DATA0	QSPIA DATA0	172	QSPIA_DATA0
QSPIA_DATA1	QSPIA DATA1	178	QSPIA_DATA1
QSPIA_DATA2	QSPIA DATA2	176	QSPIA_DATA2
QSPIA_DATA3	QSPIA DATA3	174	QSPIA_DATA3

2.9 UART

i.MX6ULL provides 8x UART (Universal Asynchronous Receiver/Transmitter), each of the UART module

supports the following serial data transmit/receive protocols and configurations:

- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none)
- Programmable baud rates up to 5 Mbps.
- 32-byte FIFO on Tx and 32 half-word FIFO on Rx

Signal	Description	Pin	Defaults Function
UART1_TXD	UART1 output	57	UART1_TXD
UART1_RXD	UART1 input	63	UART1_RXD
UART1_CTS	UART1 Clear to Send	66	UART1_CTS
UART1_RTS	UART1 Request to Send	74	UART1_RTS
UART2_TXD	UART2 output	65	UART2_TXD
UART2_RXD	UART2 input	67	UART2_RXD
UART2_CTS	UART2 Clear to Send	72	UART2_CTS
UART2_RTS	UART2 Request to Send	78	UART2_RTS
UART3_TXD	UART3 output	69	UART3_TXD
UART3_RXD	UART3 input	73	UART3_RXD
UART3_CTS	UART3 Clear to Send	76	UART3_CTS
UART3_RTS	UART3 Request to Send	80	UART3_RTS
UART4_TXD	UART4 output	75	UART4_TXD
UART4_RXD	UART4 input	77	UART4_RXD
uart4.RTS_B	UART4 Request to Send	162	LCD_VSYNC
uart4.CTS_B	UART4 Clear to Send	160	LCD_HSYNC
UART5_TXD	UART5 output	79	UART5_TXD
UART5_RXD	UART5 input	68	UART5_RXD
uart5.RTS_B	UART5 Request to Send	101	ENET1_CRS_DV
uart5.CTS_B	UART5 Clear to Send	122	ENET1_TXD0
uart6.TX	UART6 output	111	ENET2_RXD0
uart6.RX	UART6 input	113	ENET2_RXD1
uart6.CTS_B	UART6 Clear to Send	119	ENET2_TXD1
		124	ENET1_TXD1
uart6.RTS_B	UART6 Request to Send	114	ENET1_TXEN
uart7.TX	UART7 output	117	ENET2_CRS_DV
		144	LCD_DATA16
uart7.RX	UART7 input	123	ENET2_TXD0
		133	LCD_DATA17
uart7.CTS_B	UART7 Clear to Send	118	ENET1_TX_CLK
		151	LCD_DATA6
uart7.RTS_B	UART7 Request to Send	126	ENET1_RXER
		166	LCD_DATA7
uart8.TX	UART8 output	140	LCD_DATA20
uart8.RX	UART8 input	121	ENET2_TXEN
		129	LCD_DATA21
uart8.CTS_B	UART8 Clear to Send	105	ENET2_TX_CLK

Signal	Description	Pin	Defaults Function
		158	LCD_DATA4
uart8.RTS_B	UART8 Request to Send	109	ENET2_RXER
		149	LCD_DATA5

2.10 I2C

The Inter-Integrated Circuit (I2C) provides functionality of a standard I2C master and slave. The I2C is designed to be compatible with the I2C Bus Specification, version 2.1, by Philips Semiconductor (now NXP Semiconductors).

The CM6ULL features 4x I2C, supports 400 kbps.

Signal	Description	Pin	Defaults Function
I2C1_SCL	I2C1 clock	75	I2C1_SCL
I2C1_SDA	I2C1 data	77	I2C1_SDA
I2C2_SCL	I2C2 clock	79	I2C2_SCL
I2C2_SDA	I2C2 data	68	I2C2_SDA
i2c3.SCL	I2C3 clock	57	UART1_TXD
		111	ENET2_RXD0
		155	LCD_DATA1
i2c3.SDA	I2C3 data	63	UART1_RXD
		113	ENET2_RXD1
		153	LCD_DATA0
i2c4.SCL	I2C4 clock	65	UART2_TXD
		117	ENET2_CRS_DV
		154	LCD_DATA3
i2c4.SDA	I2C4 data	67	UART2_RXD
		164	LCD_DATA2
		123	ENET2_TXD0

2.11 PWM

The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound. The i.MX 6ULL features 8x PWM.

Signal	Description	Pin	Defaults Function
pwm1.OUT	PWM1 Output	97	ENET1_RXD0
		153	LCD_DATA0
pwm2.OUT	PWM2 Output	56	SD1_nRST
		99	ENET1_RXD1
		155	LCD_DATA1
pwm3.OUT	PWM3 Output	47	USB_OTG1_PWR

		164	LCD_DATA2
pwm4.OUT	PWM4 Output	49	SD1_VSELECT
		154	LCD_DATA3
		182	QSPIA_SCLK
pwm5.OUT	PWM5 Output	119	ENET2_TXD1
		124	ENET1_TXD1
		137	LCD_DATA18
		170	QSPIA_nSS0
pwm6.OUT	PWM6 Output	43	JTAG_TDI
		114	ENET1_TXEN
		138	LCD_DATA19
pwm7.OUT	PWM7 Output	54	JTAG_TCK
		118	ENET1_TX_CLK
		198	CSI_VSYNC
pwm8.OUT	PWM8 Output	126	ENET1_RXER
		197	CSI_HSYNC

2.12 JTAG

The SJC provides JTAG interface, which complies with JTAG TAP standards, to internal logic. The i.MX 6ULL processors use JTAG port for production, testing, and system debugging.

Signal	Description	Pin	Defaults Function
JTAG_MOD	Strapping: 0: Debug Mode (default, 10k pull down on module) 1: Boundary Scan Mode (overdrive it externally)	33	SPDIF_TX
JTAG_TMS	JTAG mode select	46	JTAG_TMS
JTAG_TDO	JTAG data output	52	JTAG_TDO
JTAG_TDI	JTAG data in	43	JTAG_TDI
JTAG_TCK	JTAG clock	54	JTAG_TCK
JTAG_nTRST	JTAG reset	48	JTAG_nTRST

2.13 CAN

Two Flexible Controller Area Network (FlexCAN). The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames.

Features:

- Bit rate up to 1Mb/s
- Content-related addressing
- Flexible mailboxes of eight-byte data length (configurable as RX or TX)

Signal	Description	Pin	Defaults Function
CAN1_RX	CAN1 input	80	UART3_RTS
CAN1_TX	CAN1 output	76	UART3_CTS
CAN2_RX	CAN2 input	78	UART2_RTS
CAN2_TX	CAN2 output	72	UART2_CTS

3 Product Electrical Characteristics

3.1 Dissipation and Temperature

Symbol	Parameter	Min	Typ	Max	Unit
VSYS	System Voltage	3.8	5	6	V
VCC_IO	System IO Voltage	3.3-5%	3.3	3.3+5%	V
Isys_in	VSYS input Current				mA
Ivio_out	VCC_IO output Current				mA
VCC_RTC	RTC Voltage	1.8	3	3.4	V
Iirtc	RTC input Current				uA
Ta	Operating Temperature	0	NA	70	°C
Tstg	Storage Temperature	-40	NA	85	°C

3.2 Reliability of Test

High Temperature Operating Test		
Contents	Operating 8h in high temperature	55°C±2°C
Result	Pass	

Operating Life Test		
Contents	Operating in room	120h
Result	Pass	